ADVANCED ULTRA LOW-POWER SEMICONDUCTOR DEVICES

Design and Applications

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Table of Contents

Cover

Table of Contents

Series Page

Title Page

Copyright Page

Preface

1 Subthreshold Transistors: Concept and Technology

- 1.1 Introduction
- 1.2 Major Sources of Leakage and Possible Methods of Prevention
- 1.3 Possibilities and Challenges
- 1.4 Conclusions
- References

2 Introduction to Conventional MOSFET and Advanced Transistor TFET

- 2.1 Introduction
- 2.2 Device Structure
- 2.3 TFET Principle of Operation
- 2.4 Material Characterization
- 2.5 Characteristics of TFET
- 2.6 Comparison of OFF-State Characteristics
- 2.7 Phonon Scattering’s Impact
- 2.8 ON-State Performance Comparison
- 2.9 Performance Analysis Based on Intrinsic Delay
- 2.10 Bandgap’s Effect on Device Performance
- 2.11 MOSFET and TFET Scaling Behaviour
- 2.12 Surface Potential of an N-TFET and N-MOSFET

2.13 Professional Advantages of TFET over MOSFET
2.14 Conclusion
References
3 Operation Principle and Fabrication of TFET
3.1 Introduction
3.2 Planar MOSFET’s Limitations
3.3 Demand for Low Power Operation
3.4 TFET: Operation Principle of TFET
3.5 TFET: Recent Design Issues in TFET
3.6 TFET: Modeling and Application
3.7 TFET: Fabrication Perspective
3.8 TFET: Applications and Future of Low-Power Electronics
3.9 Expected Challenges in Replacing MOSFET with TFET
3.10 Conclusion
References
4 Mathematical Modeling of TFET and Its Future Applications: Ultra Low-Power SRAM Circuit and III-IV TFET
4.1 Introduction
4.2 Modeling Approaches
4.3 Structure
4.4 Applications of Tunnel Field-Effect Transistor
4.5 Road Ahead for Tunnel Field Effect Transistors
References
5 Analysis of Channel Doping Variation on Transfer Characteristics to High Frequency Performance of F-TFET
5.1 Introduction
5.2 Simulated Device Structure and Parameters
5.3 DC Characteristics
5.4 Analysis of Analog/RF FOMs
5.5 Conclusion

References
6 Comparative Study of Gate Engineered TFETs and Optimization of Ferroelectric Heterogate TFET Structure
6.1 Introduction
6.2 Study of Different TFET Structures
6.3 Proposed Structure
6.4 Results and Discussion
6.5 Conclusion
6.6 Future Scope
References
7 State of the Art Tunnel FETs for Low Power Memory Applications
7.1 Static Random Access Memory
7.2 Performance Parameters of SRAM Cell
7.3 TFET-Based SRAM Cell Design
7.4 Conclusion
References
8 Epitaxial Layer-Based Si/SiGe Hetero-Junction Line Tunnel FETs: A Physical Insight
8.1 Fundamental Limitation of CMOS: Tunnel FETs
8.2 Working Principle of Tunnel FET
8.3 Point and Line TFETs: Tunneling Direction
8.4 Perspective of Line TFETs
8.5 Analytical Models of Line TFETs
8.6 Line TFETs for Analog & Digital Circuits Design
8.7 Other Steep Slope Devices
8.8 Conclusion
References
9 Investigation of Thermal Performance on Conventional and Junctionless Nanosheet Field Effect Transistors
9.1 Introduction

9.2 Device Simulation Details
9.3 Results and Discussion
9.4 Conclusion
Acknowledgement
References
10 Introduction to Newly Adopted NCFET and Ferroelectrics for Low-Power Application
10.1 Introduction
10.2 NCFET and Its Design Constraints
10.3 NCFET for Low-Power Applications
10.4 Summary
References
11 Application of Ferroelectrics: Monolithic-3D Inference Engine with IGZO Based Ferroelectric Thin Film Transistor Synapses
11.1 Introduction
11.2 Ferroelectricity in Hafnium Oxide
11.3 IGZO Based Ferroelectric Thin Film Transistor
11.4 Applications in Neural Networks
11.5 Conclusion
References
12 Radiation Effects and Their Impact on SRAM Design: A Comprehensive Survey with Contemporary Challenges
12.1 Introduction
12.2 Literature Survey
12.3 Impact of Radiation Effects on Sram Cells
12.4 Results and Discussion
12.5 Conclusion
Declarations
References

13 Final Summary and Future of Advanced Ultra Low Power Metal Oxide Semiconductor Field Effect Transistors
13.1 Introduction
13.2 Challenges in Future Ultra-Low Power Semiconductors
13.3 Conclusion
References
Index
Also of Interest
End User License Agreement

List of Tables

Chapter 1
Table 1.1 Impact of reverse short channel effect (RSCE) on device and circuit ...
Table 1.2 Parameter comparison between Bulk CMOS and DGSOI at equal supply vol...
Table 1.3 Impact of parameters variation in strong inversion and sub-threshold...
Chapter 3
Table 3.1 Supply voltage scaling trend at various technology nodes [8].
Table 3.2 Displays the noise margin for FinField effect transistors and tunnel...
Chapter 5
Table 5.1 Overview of critical parameters for different doping levels of chann...
Chapter 6
Table 6.1 Comparative results of memory window.
Chapter 7

Table 7.1 Summary of performance parameters of TFET and FinFET based SRAM [25]...

Table 7.2 Benchmarking between SRAM cell implementation using TFET and FinFET ...

Table 7.3 Comparison on SRAM circuits based on GaN TFET, FinFET, and graphene ...

Table 7.4 Comparison on SRAM circuits based on GaN TFET, FinFET [35].

Table 7.5 Comparison of performance parameters of proposed TFET SRAM and other...

Chapter 9

Table 9.1 Design parameters of NSFET.

Chapter 10

Table 10.1 Negative capacitance based different device structures and their pe...

Chapter 11

Table 11.1 Benchmarking table.

Chapter 13

Table 13.1 Overview of disadvantages and advantages of structure engineering....

Table 13.2 Overview of disadvantages and advantages of material engineering.

List of Illustrations

Chapter 1

Figure 1.1 Major components of leakage [8].

Figure 1.2 Threshold voltage variation with channel length and width [8, 15, 1...

Figure 1.3 Temperature effect on current [8, 13].

Figure 1.4 FN tunnelling [8].

Figure 1.5 Direct tunnelling [20].

Figure 1.6 GIDL effect on subthreshold current [24].

Figure 1.7 (a) Gate capacitance, subthreshold sope; (b) field and supply volta...

Figure 1.8 (a) Delay vs gate length of an inverter (b) Gate capacitance vs gat...

Figure 1.9 (a) Polarization in FE materials; (b) NC in MOSFETs; (c) charge vol...

Figure 1.10 Impact of NC on current, subthreshold slope, and threshold voltage...

Chapter 2

Figure 2.1 MOSFET and TFET doped region comparison.

Figure 2.2 TFET biasing scheme: (a) n-type TFET and (b) p-type TFET.

Figure 2.3 MOSFET and TFET schematic valence and conduction band diagrams.

Figure 2.4 Band profile of TFET at beginning of and deep into ON state.

Figure 2.5 TFET schematic and energy band structure.

Figure 2.6 Band diagram along surface of TFET in OFF state (i.e., at V_{GS} = 0 V...

Figure 2.7 I_D – V_G characteristics of single gate SOI-TFET.

Figure 2.8 MOSFET I_{DS}-V_{GS} temperature correlation.

Figure 2.9 I_{DS}–V_{GS} dependence on temperature in TFET.

Figure 2.10 Comparison of MOSFET and TFET’s linear IDS-VGS under dissipative a...

Figure 2.11 Comparison of intrinsic delay with I_{ON}/I_{OFF}.

Figure 2.12 Device performance under dissipative transport in bandgap-dependen...

Figure 2.13 Device performance under dissipative transport is bandgap-dependen...

Figure 2.14 SS vs. temperature comparison of MOSFET and TFET.

Figure 2.15 Drain current comparison.

Figure 2.16 Surface potential of N-TFET and N-MOSFET.

Chapter 3

Figure 3.1 Trends in supply voltage scaling and threshold voltage based on int...

Figure 3.2 TFET operation: The internal structure of the transistor, band alig...

Figure 3.3 Schematic illustration of (a) MOSFET and (b) TFET devices.

Figure 3.4 Energy band diagrams of (a) MOSFET and (b) TFET in the ON and OFF s...

Figure 3.5 Structural and functional distinctions between (a) line TFET and (b...

Figure 3.6 SS versus channel length comparison for various oxide thicknesses i...

Figure 3.7 Fabrication steps for TFET.

Chapter 4

Figure 4.1 Procedure to find drain current using analytical modeling.

Figure 4.2 2D device structure of silicon dual gate silicon tunnel field.

Figure 4.3 Distribution of surface potential along x-direction in silicon dual...

Figure 4.4 Distribution of surface potential along y-direction in silicon dual...

Figure 4.5 Drain current characteristics of silicon dual gate TFET.

Figure 4.6 2D structure of TFET with targeted biomolecules [7].

Figure 4.7 Schematic of (a) silicon nanowire-based TFET biosensor [10]; (b) di...

Figure 4.8 Structure of (a) 6T SRAM and (b) 7T SRAM [11].

Figure 4.9 3D and 2D structure of AlGaSb/GaAsP electrically doped TFET [12].

Figure 4.10 Frequency (cut-off) vs. gate voltage in TFET.

Chapter 5

Figure 5.1 2D cross-sectional representation of F-TFET with two cut-lines: AB ...

Figure 5.2 ON-state EBD at (a) Source-Channel-Interface (SCI_{int}) along XY cut-...

Figure 5.3 Ramifications of N_C on potential at (a) SCI_{int} and (b) DCI_{int}.

Figure 5.4 Variations in Electric Field (E_{fields}) for ON State at (a) SCI_{int} a...

Figure 5.5 Variations in recombination rate for ON State at (a) SCI_{int} and (b)...

Figure 5.6 I_{ds}-V_{gs} plot to analyse the effect of channel doping deviations on ...

Figure 5.7 Variations in (a) I_{ON}/I_{OFF} Ratio (Left Y-axis) and I_{ON} (Right Y-axi...

Figure 5.8 Plots of (a) C_{gd} and (b) C_{gs}.

Figure 5.9 Curves of (a) g_m and (b) f_t under N_C deviations according to gate v...

Figure 5.10 Variation in (a) GBP and (b) transit time.

Figure 5.11 Variation in (a) TFP and (b) TGF.

Chapter 6

Figure 6.1 I_{ON}/I_{OFF} for different structures.

Figure 6.2 Least subthreshold swing value for different structures.

Figure 6.3 I_D vs. V_{GS} for various ferroelectric structures.

Figure 6.4 Heterogate ferroelectric tunnel field effect transistor (HF TFET)....

Figure 6.5 Heterogate TFET-1.

Figure 6.6 Surface potential at V_{gs}=2V.

Figure 6.7 Comparison of average subthreshold swing for variants of heterogate...

Figure 6.8 Comparison of I_{ON}/I_{OFF} for variants of heterogate ferroelectric TFE...

Figure 6.9 Drain induced barrier lowering comparison between heterogate TFET a...

Figure 6.10 V_{th} dependency at varying channel doping concentration for heterog...

Figure 6.11 Bar diagram of standard deviation of threshold voltage at differen...

Figure 6.12 Temperature dependence of heterogate ferroelectric TFET.

Figure 6.13 Variation of I_d-V_{gs} characteristics due to acceptor interface trap...

Figure 6.14 Variation of I_d-V_{gs} characteristics due to donor interface trap ch...

Figure 6.15 (a) Conduction energy band deviation for acceptor (-ve) and donor ...

Figure 6.16 Variation of threshold voltage with interface trap charges.

Figure 6.17 I_d-V_g characteristics due to acceptor interface trap charges by va...

Figure 6.18 I_d-V_g Characteristics due to donor interface trap charges by varia...

Figure 6.19 I_d-V_{gs} characteristics with temperature variation at different int...

Figure 6.20 Variation of threshold voltage with interface trap charges at vari...

Figure 6.21 Variation of band diagram with temperature for 0 concentration of ...

Figure 6.22 Variation of band diagram with temperature for $-1x10^{12}$ interface t...

Figure 6.23 Variation of band diagram with temperature for $+1x10^{12}$ interface t...

Figure 6.24 Forward and reverse sweep in I_D-V_{GS}.

Figure 6.25 Modified structure of heterogate tunnel FET structure with additio...

Figure 6.26 Charge penetration through thin dielectric layer (DE).

Chapter 7

Figure 7.1 Memory hierarchy [4].

Figure 7.2 Typical structure of a 6T SRAM cell [6].

Figure 7.3 SRAM cell under read operation [6].

Figure 7.4 SRAM cell under write operation [6].

Figure 7.5 Graphical interpretation of SNM [1].

Figure 7.6 6T SRAM with varying access transistor configuration [21].

Figure 7.7 Output characteristics of p-n-p-n TFET in double gate architecture ...

Figure 7.8 Difference in current flow path in 6T CMOS and 6T TFET-based SRAM w...

Figure 7.9 6T TFET-based SRAM with outward configuration of access transistor ...

Figure 7.10 Double gate N-type and P-type Si-TFET [7].

Figure 7.11 Novel 6T-based TFET SRAM cell [7].

Figure 7.12 Working of modified TFET based 6T SRAM cell during read and write ...

Figure 7.13 (a & b) Read circuit of double gate TFET 6T SRAM cell; c) Voltage ...

Figure 7.14 (a) Write circuit of DGTFET based 6T SRAM Cell; b) Voltage levels ...

Figure 7.15 6T SRAM Cell with inward and outward configuration of access trans...

Figure 7.16 Nanowire based TFET for SRAM cell implementation [23].

Figure 7.17 (a) 6T SRAM cell implemented; (b) Layout of nanowire TFET [14].

Figure 7.18 GaSb/InAs heterojunction based vertical TFET [25].

Figure 7.19 (a) p-TFET with InGaAs/Ge heterojunction; (b) n-TFET with InGaAs/G...

Figure 7.20 7T SRAM cell with read assisted architecture [21].

Figure 7.21 7T SRAM cell design [9].

Figure 7.22 (a) SP-DGTFET; (b) DP-DGTFET [20].

Figure 7.23 7T TFET memory cell designs [20].

Figure 7.24 7T TFET SRAM with extra read transistor [7].

Figure 7.25 Device structure of GaSb/InAs heterojunction based TFET [31].

Figure 7.26 8T SRAM cell implementation using TFETs [31].

Figure 7.27 (a) n Channel FET; (b) n-type p-n-p-n based TFET structure; (c) p ...

Figure 7.28 (a) MOSFET based 8T SRAM; (b) TFET based 8T SRAM; (c) TFET based 7...

Figure 7.29 (a) 6T SRAM; (b) 8T SRAM cell design [32].

Figure 7.30 8T SRAM cell design [33].

Figure 7.31 8T SRAM cell design using GaN TFET [35].

Figure 7.32 Combinational access 10T SRAM cell [42].

Figure 7.33 (a) 10T SRAM cell design; (b) signals during operation [8].

Figure 7.34 (a) Hold state; (b) Read operation; (c) Write operation of Bit “1”...

Figure 7.35 4T TFET based SRAM cell [43].

Figure 7.36 Storing the bit [44].

Figure 7.37 Writing the bit [44].

Figure 7.38 Reading a bit [44].

Figure 7.39 Proposed 3T TFET based SRAM cell [13].

Chapter 8

Figure 8.1 (a) Transfer characteristics of MOSFET indicating an exponential in...

Figure 8.2 Comparison of working mechanism between MOSFET and TFET. E_C, E_V, an...

Figure 8.3 Classification of TFETs per direction of tunneling. Solid arrows in...

Figure 8.4 Current density in line and point TFET devices obtained through num...

Figure 8.5 (a) Structure of fabricated L-TFET; (b) Energy band offset at heter...

Figure 8.6 Transfer characteristics of counter-doped source pocket-based L-FET...

Figure 8.7 (a) 2-D schematic of fabricated device; (b) Band offset at Hetero-j...

Figure 8.8 3D/2D cross-section of Fin-shaped line tunnel FET; (b) Typical proc...

Figure 8.9 (a) Three-dimensional schematic of area-scaled NS-TFET; (b) Transfe...

Figure 8.10 (a) Stacked nanosheet line TFET with 3 sheets; (b) Cross-section a...

Figure 8.11 (a) Estimating constant gate-drain bias from gate capacitance curv...

Figure 8.12 (a) Line TFET-based current mirror circuit; (b) Current ratio in i...

Chapter 9

Figure 9.1 3-dimensional view of NSFET.

Figure 9.2 Matching of simulated data with experimental data [51].

Figure 9.3 I_d-V_g characteristics: (a) CL NSFET; (b) JL NSFET.

Figure 9.4 g_m/I_d plots: (a) CL NSFET; (b) JL NSFET.

Figure 9.5 Analog/RF parameters of CL and JL NSFET with respect to temperature...

Figure 9.6 Id-Vg characteristics of different dielectrics at various temperatu...

Figure 9.7 gm/Id plots of different dielectrics at various temperatures: (a) C...

Figure 9.8 Analog/RF parameters of CL and JL NSFET with respect to temperature...

Figure 9.9 I_d-V_g characteristics of different spacer dielectrics at various te...

Figure 9.10 gm/Id plots of different spacer dielectrics at various temperature...

Figure 9.11 Analog/RF parameters of CL and JL NSFET in conjunction with temper...

Chapter 10

Figure 10.1 Basic structure of Negative Capacitance FET (NCFET) [26].

Figure 10.2 I-V characteristics of NCFETs vs. conventional MOSFETs [27].

Figure 10.3 Types of NCFET structures: (a) Metal-Ferroelectric-Insulator-Semic...

Figure 10.4 Equivalent capacitance model related to NCFETs [17].

Figure 10.5 Distinct spacer configurations: (a) Air, (b) Fin Selective, (c) Fi...

Figure 10.6 Variation of GIDL current with ferroelectric thickness in NC-FinFE...

Chapter 11

Figure 11.1 Schematic representation of a multi-layer perceptron neural networ...

Figure 11.2 Schematic representation of VGG-16 convolutional neural network.

Figure 11.3 Historical timeline and major milestones in research of neural net...

Figure 11.4 Crystallographic phases and their unit-cells in Quasi-cubic repres...

Figure 11.5 Transmission Kikuchi Diffraction (TKD) phase map images of Si- and...

Figure 11.6 Schematic representation of stress dependence of Hafnium oxide. Fi...

Figure 11.7 Process flow for fabricating IGZO-based FeTFT.

Figure 11.8 Transfer Characteristics of FeTFTs with 30 nm IGZO. Partial switch...

Figure 11.9 Architecture of proposed monolithic 3D-inference engine.

Figure 11.10 Comparison of FeTFT devices with other *State-of-Art* synaptic devi...

Chapter 12

Figure 12.1 Subthreshold SRAM operational effects and improvement methods.

Figure 12.2 Comparative analysis of radiation hardened 12TSRAM cells: RHPD12T ...

Figure 12.3 Comparative analysis of radiation hardened 10TSRAM cells: RHBD10T ...

Figure 12.4 Transient simulation of 6T SRAM cell [49] with SEU induced at 16.5...

Figure 12.5 Effect of SEU on 6T SRAM CELL operating with supply voltage (VDD=0...

Figure 12.6 Effect of SEU on RHBD10T SRAM CELL [29] operating with supply volt...

Figure 12.7 Effect of SEU on Nwise10T SRAM CELL [8] operating with supply volt...

Figure 12.8 Effect of SEU on WL and BL boosted 10T SRAM CELL [3] operating wit...

Figure 12.9 Effect of SEU on QCCE 10T SRAM CELL [28] operating with supply vol...

Figure 12.10 Effect of SEU on RHBD 12T SRAM CELL [29] operating with supply vo...

Figure 12.11 Effect of SEU on QCCE 12T SRAM CELL [28] operating with supply vo...

Figure 12.12 Transient simulation of low leakage SEU immune. 12T SRAM Cell [39...

Figure 12.13 Transient simulation of 12T SRAM Cell [38] with SEU induced and o...

Chapter 13

Figure 13.1 Structure evolution of transistor (from planar MOSFET, via FinFET,...

Figure 13.2 Material evolution of transistor.

Figure 13.3 Step-by-step fabrication process of vertically stacked GAA MOSFET ...

Figure 13.4 Fabrication process of heterogate dielectric structure.

Figure 13.5 Example of Semiconductor Process: Wet Etching (This photo was take...

Figure 13.6 Example of Semiconductor Process: Oxidation, Chemical Vapor Deposi...

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Preface

Recently, the advent of portable electronic devices (Apple iPhone, Apple Watch, Galaxy Watch, Galaxy Gear) and social media platforms (TikTok, Instagram, Facebook) has revolutionized the modern information technology (IT) market. Since we are now living in an extremely mobile society, we cannot only make and receive calls anytime but also send and receive photos and videos anytime, no matter where we are. Nowadays, many people are also looking at their phones when they are taking subways, buses, trains, and even airplanes.

For these reasons, there have been steady demands for low-power semiconductor design so that low power consumption can be realized in electronic devices. In particular, the advent of electronic watches, driverless cars (unmanned vehicles), drones, and artificial intelligence (AI) requires further low power consumption, or '*ultra-low power consumption*', so that people can use portable electronic devices for longer.

In this regard, the design of an '*ultra-low power semiconductor*' is essential and will be paramount in future semiconductor design. In this book, several state-of-the-art technologies have been carefully selected and introduced, including tunnel field-effect transistors (TFET), fin-shaped field-effect transistors (FinFET), gate-all-around (GAA) MOSFET, nanosheet field-effect transistors (NSFET), static random-access memory (SRAM), and negative capacitance field-effect transistors (NCFET).

This book is a selective collection of recent cutting-edge technologies that have been suggested for future ultra-low power semiconductor design. Several intuitive graphical images and mathematical equations have been carefully presented so that non-IT majors can also easily understand the contents. This book may be used as teaching material for undergraduate (especially for 3rd and 4th year students) and post-graduate course work, as well as for advanced researchers working in several engineering industries.

Shubham Tayal, Shiromani Balmukund Rahi, Abhishek Kumar Upadhyay, and Young Suh Song

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1
Subthreshold Transistors: Concept and Technology

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Abstract

The continuous downscaling of Si MOS transistors facilitated technology to follow Moor's Law which states that transistor density doubles every 18 months. However, the fundamental material limitation of Si, popularly known as Boltzmann's tyranny, sets a limit on the subthreshold swing up to 60mV/ decade, which means the minimum voltage required for a decade of change in the current is 60 mV. In addition, the various short channel effects, including V_T roll-off, increasing I_{OFF}, DIBL, and GIDL, also increase with downscaling. These two effects decrease the I_{ON}/I_{OFF} ratio and increase the power dissipation in the transistor, which is very significant, particularly in sub-nanometre technology. So, it is pertinent to think about applications where subthreshold current can be utilized, particularly in ultra-low power and very low-power applications. In the past few years, subthreshold region operation has gained attention and encouraging results have been reported. The presented chapter deals with the scope, challenges, and possible solutions for subthreshold transistors. It also presents developments in the recent past, new devices, structures, and materials with better subthreshold performance, such as high-k transistors, transistors on SOI, thin film transistors, multi-gate transistors, FinFETs, gate-all-around transistors, nanowire, Nano sheet, and TFETs. Recently, NCFET also reported it promises to improve subthreshold performance without changing the conventional structure of the transistor, which is encouraging.

***Keywords*:** Subthreshold transistor, tunnel FET, NC FET, scaling

1.1 Introduction

The market for power-efficient systems, such as personal digital assistants, cellular phones, and other communication devices, has grown significantly due to the fast growth of battery-operated portable applications. To meet the demand, the size of the transistor and supply voltages are scaled down. But, as the size of the transistor is getting smaller at every technology node to increase functionality and high performance, various leakages, such as sub-threshold leakage current increase, gate leakage, and band-to-band tunneling (BTBT) currents through source/drain-substrate junctions are also increasing. These leakages deteriorate device performance and inhibit further downscaling. To overcome these issues, exhaustive research has been carried out in the past that is still going on, such as a reduction in switching frequency and the development of new architectures for pipelining, connections, and logic optimization. Unfortunately, this is not sufficient for future demands for ultra-low power applications below Giga Hertz frequency applications, e.g., instruments used in medical and portable applications. Therefore, various design techniques have been proposed for power-efficient applications and subthreshold transistors are one of them. The subthreshold transistors, as the name suggests, are operated below the threshold voltage or in the subthreshold region [1–4]. The subthreshold current, which is known as the leakage current in conventional terms, can be used for ultra-low power applications. In the subthreshold region, transistors have ideal voltage transfer characteristics, high trans-conductance, and lower gate input capacitance compared to the inversion region and are therefore better for logic circuits. It provides power efficiency at the cost of performance and can be a future choice for ultra-low-power digital and memory applications [5–7]. This chapter is organized as follows. In Section 1.2, the major sources of subthreshold leakage and their possible methods of prevention are analyzed. Various challenging issues confronting the current and future robust subthreshold circuit design are discussed and the scope of subthreshold technology is also presented in Section 1.3. Finally, conclusions are drawn in Section 1.4.

1.2 Major Sources of Leakage and Possible Methods of Prevention

1.2.1 Leakage Mechanisms in MOS Transistors

In Figure 1.1 the various sources of leakage are shown: reverse-bias PN junction leakage (I_1); subthreshold leakage (I_2); oxide tunneling current (I_3); gate current due to hot-carrier injection (I_4); GIDL (I_5); and channel punch through current (I_6). The leakage current components in 2, 5, and 6 are offstate leakage mechanisms, 1 and 3 occur in both ON and OFF states, and 4 occurs in the OFF state.

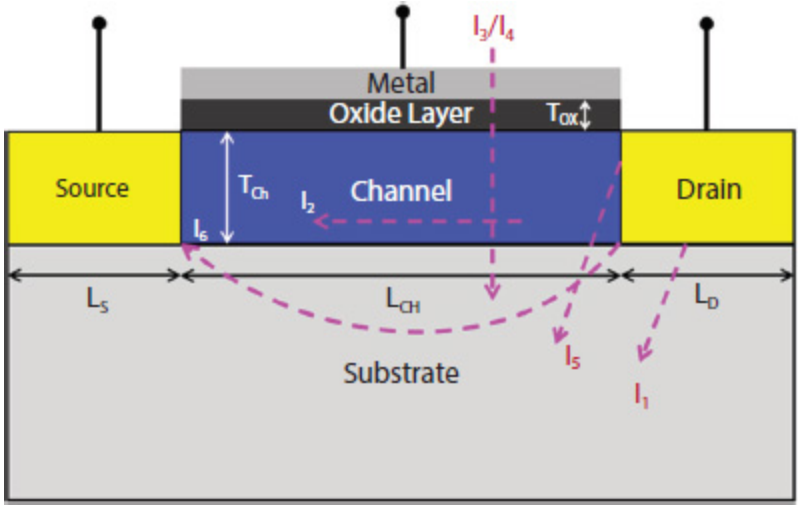

Figure 1.1 Major components of leakage [8].

1.2.1.1 Current I_1

This current is due to leakage through reverse-biased drain/source PN junctions and electron-hole pair generation in the depletion region. Additionally, leakage also occurs through overlapping gates to the drainwell PN junctions or carrier generation in drain-to-well depletion regions. Shallow junctions with high doping are used to overcome this leakage, but it also enhances band-to-band tunneling (BTBT) leakage [9].

1.2.1.1.1 Band-to-Band Tunnelling (BTBT) Current

The electric field increases up to 10^6 V/cm due to heavily doped shallow junctions, which facilitate quantum mechanical band-to-band tunneling (BTBT) across the reverse-biased PN junction and, therefore, tunneling leakage increases. Considering the step junction, the mathematical expression for tunneling current density is as follows [9]:

$$J_{BTBT} = P\frac{EV_{RB}}{\sqrt{E_G}}e^{-Q\frac{3\sqrt{E_G}}{E}}$$

$$A = \frac{\sqrt{2m^* q^3}}{4\pi^3\hbar^2}, B = \frac{4\sqrt{2m^*}}{3q\hbar}, E_G = \sqrt{\frac{2N_A N_D(V_{RB}+V_{bi})}{\varepsilon_{Si}(N_A+N_D)}}$$

where q, h, m*, E_G, V_{RB}, E, N_A, N_D, and V_{bi} are electronic charge, Planck's constant, effective mass of electron, energy-band gap, applied reverse bias, electric field at the junction doping on the p side, doping on the n side, permittivity of silicon, and built-in voltage across the junction, respectively. In state-of-the-art technology, smaller node devices are used where abrupt and high doping concentration profiles are used and therefore, BTBT leakage through the drain-well junction is high.

1.2.1.2 Current I_2

Above the threshold, voltage channel is said to be fully inverted and its concentration is compared to the bulk concentration, while below the threshold voltage, the channel is not fully inverted, but the channel has some charge and it is weakly inverted. Therefore, the leakage current varies exponentially with gate voltage flows in the device. This current is primarily diffusion current because most of the voltage drop occurs across the drain substrate PN junction, which is inherently reverse-biased. So, the vertical and horizontal fields in the channel do not vary significantly and the drift current is less compared to the diffusion current, unlike in the strong inversion region where the drift current dominates over the diffusion current. The mathematical expression of the subthreshold leakage current is as follows [10]:

$$I_{DS} = \mu_0 C_{OX}\frac{W}{L}(\eta-1)V_T{}^2 e^{\frac{V_G-V_{TH}}{\eta V_T}}(1-e^{V_{DS}/V_T})$$

$$\eta = 1+\frac{C_D}{C_{OX}} = 1+\frac{3T_{OX}}{T_D}$$

where V_{TH}, V_T, C_{OX}, μ_0, ή, T_D, C_D, and T_{OX} are the threshold voltage, thermal voltage, gate oxide capacitance, zero bias mobility, body effect coefficient, maximum depletion layer width, depletion layer capacitance, and the thickness of the gate oxide. Another important parameter in the sub-threshold region is the subthreshold slope, which indicates the speed of turning off the transistor below the threshold voltage and is given by [10].

$$S_S = \left(\frac{d(\log_{10} I_{DS})}{dV_{GS}} \right)^{-1} = 2.3 \frac{kT}{q} \left(1 + \frac{C_D}{C_{OX}} \right) = 2.3\eta \frac{kT}{q}$$

The lower the value of SS, the better the device is. At 300 K, its minimum value is 60mV/decade. As suggested by the expression, the lower value can be obtained by reducing temperature T, higher C_{ox} or a thinner oxide layer, and lower C_{dm} or a thicker depletion layer or lower substrate doping.

1.2.1.2.1 DIBL (Drain-Induced Barrier Lowering)

Ideally, the drain voltage should have a minimum effect on the source-channel barrier or the threshold voltage of the MOSFETs.

In real devices, particularly the short-channel ones, drain voltage affects the channel conduction and the barrier between the source and channel at high drain voltage. This is known as the drain induced barrier-lowering phenomenon and thus, the drain voltage directly affects the threshold voltage along with the gate voltage. The shorter the device, the greater the impact of DIBL. Therefore, this increases the subthreshold leakage and lowers the subthreshold slope significantly as we go to smaller nodes [11]. To reduce DIBL, shallow junctions at the source and drain and higher channel doping are used [11–13].

1.2.1.2.2 Effect of Body Bias

As the expression of threshold voltage indicates, it increases with increasing reverse body bias and therefore, the off current decreases.

$$V_{TH} = V_{FB} + 2\psi + \sqrt{\frac{2q\varepsilon_{Si} N_A (2\psi + V_{BS})}{C_{OX}}}$$

where V_{TH}, V_{FB}, N_A, Ψ, V_{BS}, and, ή are threshold voltage, flat-band voltage, doping density in the substrate, difference between the Fermi potential and the intrinsic potential in the substrate, and substrate sensitivity. The expression of subthreshold leakage including weak inversion, DIBL, and body effect is as follows [14]:

$$I_{SL} = B\left(e^{\frac{1}{\eta V_T (V_{GS} - V_{TH0} - \alpha V_S + \beta V_{DS})}}\right)\left(1 - e^{\frac{v_{DS}}{V_T}}\right)$$

$$B = \mu_0 C_{OX} \frac{W}{L'} V_T{}^2 e^{\left(1.8 - \frac{\Delta V_{TH}}{\lambda V_T}\right)}$$

V_{TH0} is the zero bias threshold voltage and V_T is the thermal voltage. The effect of body bias for small voltage is linear and $\alpha V_S \alpha$ is the linearized body effect coefficient. λ is the DIBL coefficient, C_{OX} is the gate oxide capacitance, μ_0 is the zero-bias mobility, and m is the subthreshold swing coefficient of the transistor. ΔV_{TH} is a term introduced to account for transistor-to-transistor leakage variations.

1.2.1.2.3 Effect of Width Narrowing

The effect of the gate-narrowing effect can be expressed as follows:

$$V_{TH} = V_{FB} + \psi_S + \frac{Q_{BK}}{C_{OX}}$$

where V_{TH}, C_{ox}, V_{FB}, Q_{BK}, and Ψ_s are threshold voltage, capacitance across the oxide, flat band voltage, depletion charge in bulk, and surface potential. The Q_{BK} increases due to gate narrowing and therefore, V_{TH} also increases [15]. The narrower the gate width, the higher the Q_{BK} and threshold voltage of a transistor and eventually, the subthreshold leakage decreases.

1.2.1.2.4 Channel Length Variation and V_{th} Roll-Off

The reduction in threshold voltage with a reduction in channel length is termed as V_{th} roll-off. In long channel devices, the electric field is 1D, but

in short, in devices where the distance between the source and drain is comparable to the vertical depletion width, it is 2D.

It is more pronounced in depletion regions near the source and drains and therefore, lesser gate voltage is required for inversion and threshold voltage is reduced (Figure 1.2) [16–18]. The reduced threshold voltage causes more subthreshold current leakage.

1.2.1.2.5 Impact of Temperature Change

The threshold voltage of MOSFET decreases as temperature increases, therefore the subthreshold leakage current and subthreshold slope also increase (Figure 1.3). So, the applications at elevated temperatures cause significant power loss.

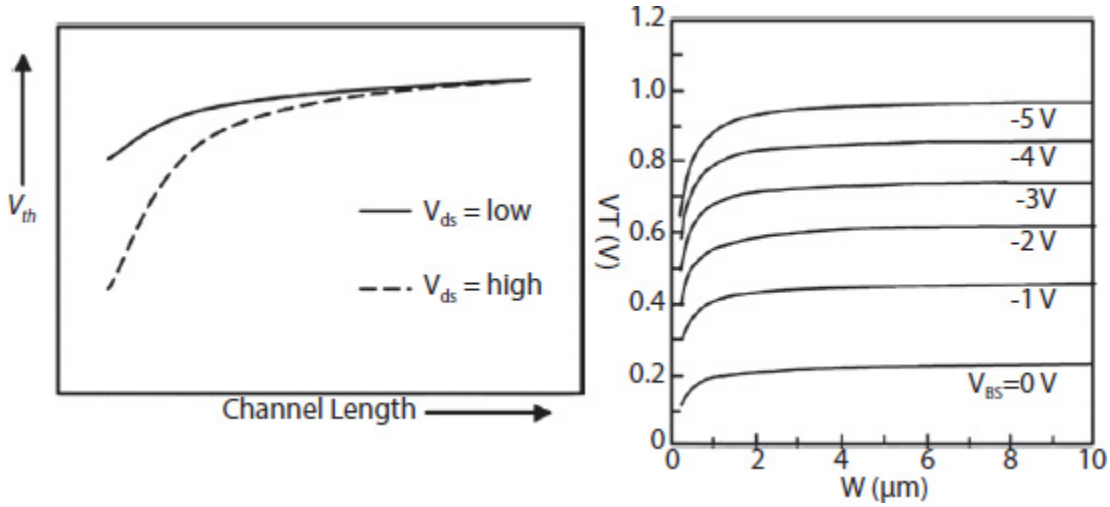

Figure 1.2 Threshold voltage variation with channel length and width [8, 15, 17].

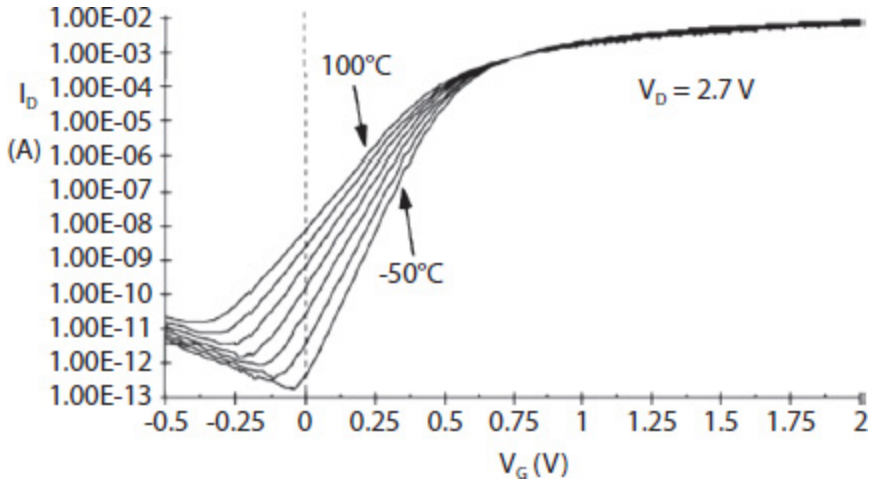

Figure 1.3 Temperature effect on current [8, 13].

1.2.1.3 Current I_3

Leakage through gate oxide occurs through the tunneling of electrons. The thinner the gate oxide layer the more tunneling there will be due to an increased electric field across the oxide, therefore causing leakage. The tunneling current is proportional to the tunneling probability of electrons. Fowler–Nordheim (FN) tunneling and direct tunneling are the two primary causes of tunneling leakage in MOSFETs. The expression for FN tunneling is [19]:

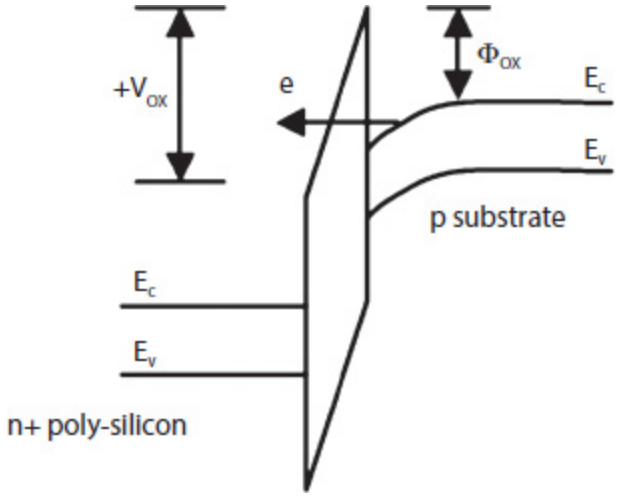

Figure 1.4 FN tunnelling [8].

$$J_{FNT} = \frac{q3E^2_{OX}}{16\pi 2\hbar\phi_{OX}} e^{\left(\frac{4\sqrt{2m^*3\sqrt{\phi_{OX}}}}{3q\hbar E_{OX}} \right)}$$

where m*, E_{OX}, $Ø_{OX}$, and V_{OX} are the effective mass of an electron in the conduction band of silicon, the field across the oxide, the barrier height for electrons in the conduction band, and the voltage drop across the oxide.

As the Figure 1.4 shows, the tunneling of electrons occurs through a triangular potential barrier ($V_{OX} > Ø_{OX}$) into the conduction band of the oxide layer. (Ignoring the effect of finite temperature and image-force-induced barrier lowering.) FN tunneling is insignificant in short-channel devices.

1.2.1.3.1 Direct Tunnelling

In a thinner oxide layer, the tunneling of electrons occurs through a trapezoidal potential barrier ($V_{OX} < Ø_{OX}$) directly from the inverted silicon surface to the gate, as shown in Figure 1.5 [20]. The direct tunneling current is significant in thin oxide layer MOSFETs and is given as [20]:

$$J_{DT} = RE^2_{OX} e^{\left(-\frac{S\left\{1-\left(1-\frac{V_{OX}}{\varphi_{OX}}\right)^{3/2}\right\}}{E_{OX}} \right)}$$

$$R = \frac{q^3}{16\pi^2\hbar\Phi_{OX}}, S = \frac{4\sqrt{2m^*}\varphi^{1.5}_{ox}}{3q\hbar}$$

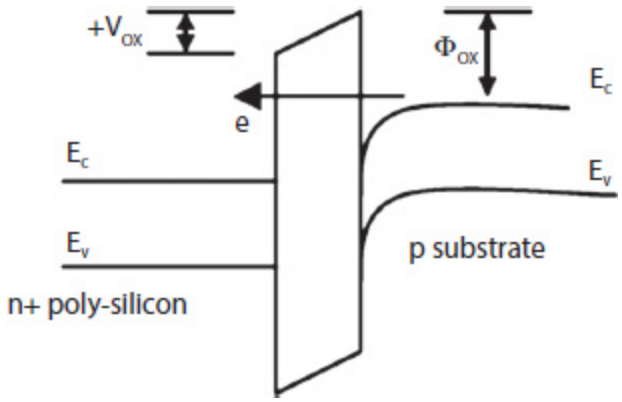

Figure 1.5 Direct tunnelling [20].

1.2.1.4 Current I_4

The hot electron injection from the substrate to the gate oxide is another leakage due to direct tunneling. In a short-channel transistor, the electric field is high near the Si–SiO_2 interface, therefore electrons gain sufficient energy to cross the interface potential barrier and enter the oxide layer. This phenomenon is known as hot-carrier injection [21].

1.2.1.5 Current I_5

Gate-Induced Drain Leakage, or GIDL, is another high field effect leakage near the drain in MOSFETs. When the gate is biased in the accumulation region, the hole concentration near the surface increases, causing a narrower depletion layer and an increased local electric field near the surface compared to elsewhere [22]. Now, at high negative gate bias or when the gate is at negative/zero voltage and the drain is at high/supply voltage, the highly n-doped drain region under the gate can be depleted/inverted, causing avalanche multiplication and BTBT due to increased field crowding and peak field [22]. The probability of tunneling through near-surface traps increases too. Due to these effects, minority carriers are emitted in the drain depletion region underneath the gate and are swept laterally to the substrate, forming a path for the GIDL [23, 24]. The increment in the electric field by using thinner oxide or higher potential between the gate and drain enhances GIDL. For very high doped drains, the depletion width and, therefore, the tunneling volume decreases, causing less GIDL. Therefore, a very high and abruptly doped drain is preferred for minimizing GIDL [21–24].

1.2.1.6 Current I_6

In state-of-the-art devices, at high reverse biased S/D junctions, the merging of the S/D depletion regions is known as punch through [24]. A drain voltage beyond the value required to establish the punch through lowers the potential barrier for the majority carriers in the source and the sub-threshold current increases (Figure 1.6). It degrades the subthreshold slope too. Punch-through is directly proportional to substrate doping, channel length, and junction width. Therefore, a halo implant at the leading edges of the

drain and source junctions is performed to reduce the punch-through effect [24].

1.2.2 Leakage Reduction Techniques

Low-voltage circuits need to be power efficient, so reduction of the leakage power in both the active and standby modes of the operation is essential. It can be achieved using both process and circuit-level techniques. In the former, leakage reduction can be achieved by controlling the dimensions of the device, such as length, oxide thickness, junction depth, etc., and the doping profile, and in the latter, threshold voltage and leakage current are controlled by controlling the voltages of different device terminals such as drain, source, gate, and body.

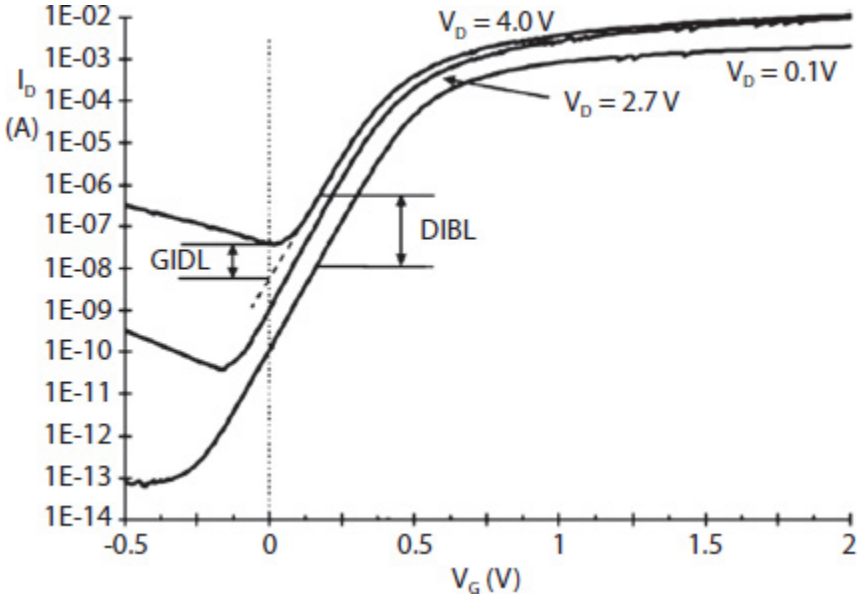

Figure 1.6 GIDL effect on subthreshold current [24].

1.2.2.1 Leakage Reduction by Channel Processing

For keeping SCE under control, the electric field is kept constant [4]. This can be achieved by scaling down the vertical dimensions of the transistor, such as gate insulator thickness and junction depth, along with the horizontal dimensions, while decreasing the applied voltages proportionally. This ensures the reliability of the scaled device in terms of hot-carrier injection. Besides changing the doping profile in the channel region, using techniques such as retrograde doping or halo implant changes the electric

field and potential distributions in the channel and thus are helpful in OFF state leakage [7–10].

1.2.2.1.1 Retrograde Doping

Non-uniform vertical retrograde channel doping is done by creating a low surface channel concentration followed by a highly doped subsurface region. Channel impurity scattering reduces in the low doping region, therefore carrier mobility increases, while the highly doped subsurface region acts as a barrier against punch through [25, 26].

1.2.2.1.2 Halo Doping

Halo doping, non-uniform channel doping in the lateral direction, is an effective way to control the threshold voltage variation with channel length. In this, p-type regions with higher doping are introduced near the source and drain end of the n-channel transistor [27]. The presence of a higher doped p-type substrate near the source/drain reduces the charge-sharing effects from the source and drain fields and therefore reduces the threshold voltage degradation due to channel length reduction. Now, the threshold voltage vs. channel length curve becomes flatter and the off-current becomes less sensitive to channel length variation. The halo implant also reduces DIBL and punch through by reducing the drain and source junction depletion region width. The price paid for this is higher BTBT and GIDL near the high field drain region [25].

1.2.2.2 Leakage Reduction Through Different Circuit Techniques

Transistor stacking, multiple threshold voltage, dynamic threshold voltage, and supply voltage scaling are the major circuit design techniques for leakage reduction in digital circuits.

1.2.2.2.1 Self-Reverse Bias Technique

Subthreshold leakage through a stack of series-connected transistors reduces due to the stacking effect, that is when more than one transistor in the stack is turned off [28–31].

1.2.2.2.2 Multiple Threshold Voltage Designs Technique

In multiple-threshold CMOS technologies, the high- and low-threshold voltage transistors are used to suppress the subthreshold leakage current and achieve high performance, respectively. These can be achieved by non-uniform channel doping [31], variations in gate oxide thickness [32], multiple channel lengths [33], or by using multiple body bias [33]. These techniques are used to design multi-threshold-voltage CMOS (MTCMOS), dual-threshold CMOS, variable threshold CMOS (VTCMOS), and dynamic threshold CMOS, which are used to control leakage and for achieving high performance according to the circuits or applications [34–37].

1.2.2.3 Scaling of Supply Voltage

Supply voltage scaling is an effective way for switching power reduction because of the quadratic dependence of switching power on the supply voltage. It also reduces the decrease in subthreshold leakage due to DIB decreases [38, 39]. There are two ways of lowering the supply voltage: static and dynamic supply scaling. In the former, multiple supply voltages are used. For high-speed requirements, high-supply voltages, and low-speed circuits, low supply voltages are used [40]. In dynamic supply scaling, the highest supply voltage delivers the highest performance at the highest frequency of operation and when the demand is low, the supply voltage and clock frequency are lowered, therefore delivering reduced performance with substantial power reduction [41].

1.3 Possibilities and Challenges

The conventional MOSFETs work as a switch in the saturation (ON state) or strong inversion region and cut-off (OFF state) regions, while subthreshold transistors work in either subthreshold or weak inversion (ON state) and cut-off (OFF state) regions. Due to reduced supply voltage, the power consumption is reduced considerably, resulting in a more power-efficient device for low-power applications. Moreover, the exponential current-voltage relationship and the logic gates made of subthreshold transistors have better voltage transfer characteristics than conventional MOSFETs. In addition, the input capacitance in subthreshold transistors is lower than in conventional MOSFETs and it consumes less power at the same frequency of operation [10]. However, due to the smaller current, it cannot be used at higher frequencies like the conventional MOSFETS. So,

possible areas for such transistors are related to ultra-low power and low frequencies or low-speed applications, such as personal digital assistants (PDA), laptops, etc. There are some applications where high-performance periods are low compared to low-performance applications and subthreshold transistors are suitable for such burst-type applications.

Despite several advantages, the market feasibility and acceptability of these transistors must go a long way in comparison to the established conventional MOSFET technology, particularly in device circuits and architecture design. One of the major challenges is to design long-life subthreshold logic gates with a considerable frequency range. The variation in device characteristics due to temperature, voltage, and process, particularly in weak inversion regions, is more due to exponential dependence and therefore, needs to be addressed urgently [42–46]. The pros and cons of device size scaling have been studied exhaustively for conventional MOSFETs, but not for subthreshold transistors. Similarly, the models for such scaling and its impact on threshold voltage and other variations must be studied for making it a potential candidate for ultra-low power applications [47–49]. Semiconductor memories have a large market, particularly for SRAM, which has high density but is very sensitive to process and other variations. This could be even worse for small-sized subthreshold transistors, so efforts must be made. In addition, the smaller I_{ON}/I_{OFF} causes difficulties in memory write and read operations.

To check the performance and variations with respect to parameters such as power, delay, etc., of a device, some standard circuits or standards are needed. Unfortunately, there are very few subthreshold operating devices/circuits that have been reported, so some international standards must be defined to compare the performances of the new devices. Similarly, new simulation tools are to be developed for better compatibility with the subthreshold technology.

Often, a system has both high and low-performance devices needing high and low currents, respectively. Since sub-threshold devices are suitable for low-current applications, their integration with high-current devices or switching of the device from strong inversion to weak inversion will be needed according to the requirement. So, very flexible or dynamic voltage scaling is required for combining low and high-performance devices [50, 51].

The CMOS technology is well-optimized for all regions of operations, but sub-threshold transistor technology is not mature enough so devicelevel optimization is necessary. The common methodologies used for device optimization are reducing SCEs, such as DIBL, punch through, and subthreshold slope, halo implant, and retrograde doping in conventional MOS technology. Since the electric field is weaker in subthreshold devices, the impact of SCEs, DIBL, punch-through, halo doping, and retrograde doping may not be essential for device optimization. This reduces fabrication cost and complexity. In addition, the junction capacitance and delay are also reduced. It is reported that the junction capacitance and power delay product become half compared to the standard device after channel doping profile optimization.

Oxide thickness optimization is crucial for conventional as well as sub-threshold transistors for better performance, but they behave differently with respect to oxide thickness variation. In conventional MOSFETs, the gate capacitance is dominated by oxide capacitance in a strong inversion region, so a minimum oxide thickness is required for a better subthreshold slope. In the subthreshold region, the net gate capacitance is comprised of intrinsic depletion, fringe, and overlap capacitances and the variation of these capacitances with respect to oxide thickness is different. For example, the fringe and overlap capacitances vary logarithmically and inversely with respect to oxide thickness. Figure 1.7a shows that the behaviors of subthreshold swing and net gate capacitance are opposite with respect to oxide thickness variations. Similarly, from Figure 1.7b, for a fixed value of current, the requirement of supply voltage decreases with oxide thickness but increases after a minimum point. So, careful oxide thickness optimization is necessary for better capacitance and subthreshold swing [52].

Threshold voltage roll-off phenomenon is significant in short-channel MOSFETs and gets worse when combined with DIBL. To mitigate its effect, a halo implant is done in conventional devices and a reverse short channel effect is observed where threshold voltage decreases as channel length increases, known as a reverse short channel effect (RSCE). RSCE is more effective in subthreshold transistors compared to SCE and allows using longer channel devices with improved drive current without increasing the capacitance. Therefore, RSCE improves performances such

as capacitance, drive current, and subthreshold swing of subthreshold transistors, as shown in Table 1.1 [12].

The conventional device sizing paradigm is based on the current-voltage relationship in the strong inversion region and, therefore, in logical effort calculations the width ratio of PMOS and NMOS is 2.5 (mobility ratio of electrons and holes) for equal currents. However, the current-voltage relationship in subthreshold transistors is different and a new device sizing paradigm must be adopted. The width ratio of PMOS and NMOS has been found to be 1.5 for equal rise and fall delays at the same supply voltage.

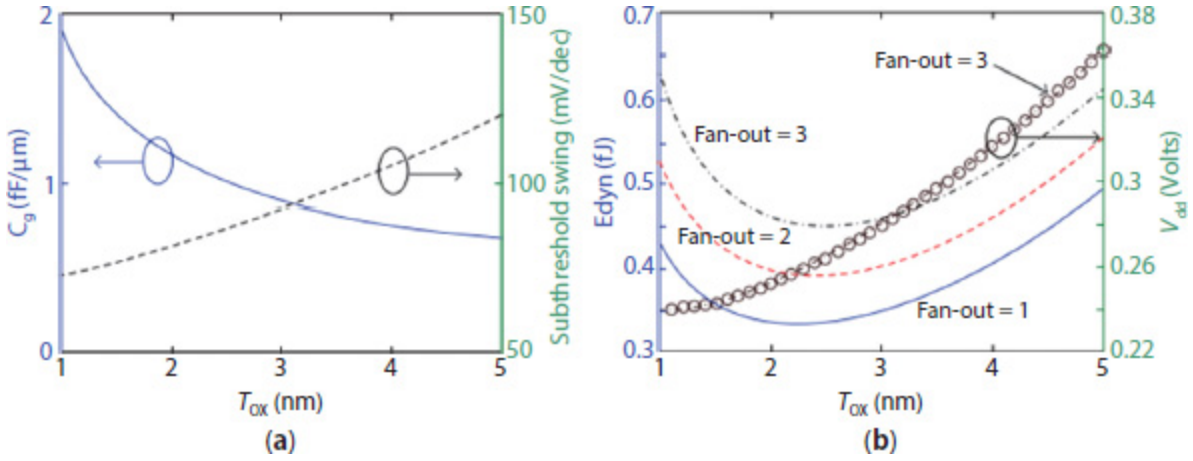

Figure 1.7 (a) Gate capacitance, subthreshold sope; (b) field and supply voltage, variation with oxide thickness [52].

Table 1.1 Impact of reverse short channel effect (RSCE) on device and circuit performance [12].

Parameter	At the device level	At the circuit-level
S (mV/dec)	71 (16 mV1 ss)	—
I_{ON}/I_{OFF}	2.5X improvement	—
Device capacitance	Low	—
Process variations	—	Reduce
Avg. delay	—	13% improvement
Avg. power	—	31% reduction
Op. frequency	—	100 MHz
PDP (energy)	—	40% reduction

The performance of multiple gate MOSFETs and TFETs [53–65] for subthreshold region operations has been proven to be encouraging [53, 54]. The double gate provides better control over the channel and therefore, on current conduction in inversion, as well as the subthreshold region of operations. This gives better subthreshold slope, lower junction capacitance, resiliency to variations in gate length, oxide thickness, etc. and thus enhances performance for low-power and high-performance circuits with better scalability [53–65]. The salient features of multiple-gate MOS technology are discussed below. Figure 1.8a shows that the delay decreases with gate length, but after a certain point it does not change much with gate length. So, a larger gate length can be used without much compromise in delay for the inverter.

Figure 1.8b shows that in the subthreshold region, the variation of the gate capacitance is negligible (the overlap and fringe capacitance dominate in this region of operation and do not vary much with gate length) for DG n-channel MOSFET. As the intrinsic capacitance is negligible in the sub-threshold region, the total gate capacitance is a combination of overlap and fringe capacitances. Therefore, from Figure 1.8, it can be concluded that a longer device can be used with better ON current, delay, and subthreshold slope without much compromise in the device performance (see Figure 1.8c). In addition, SCEs are less prominent in longer devices [65].

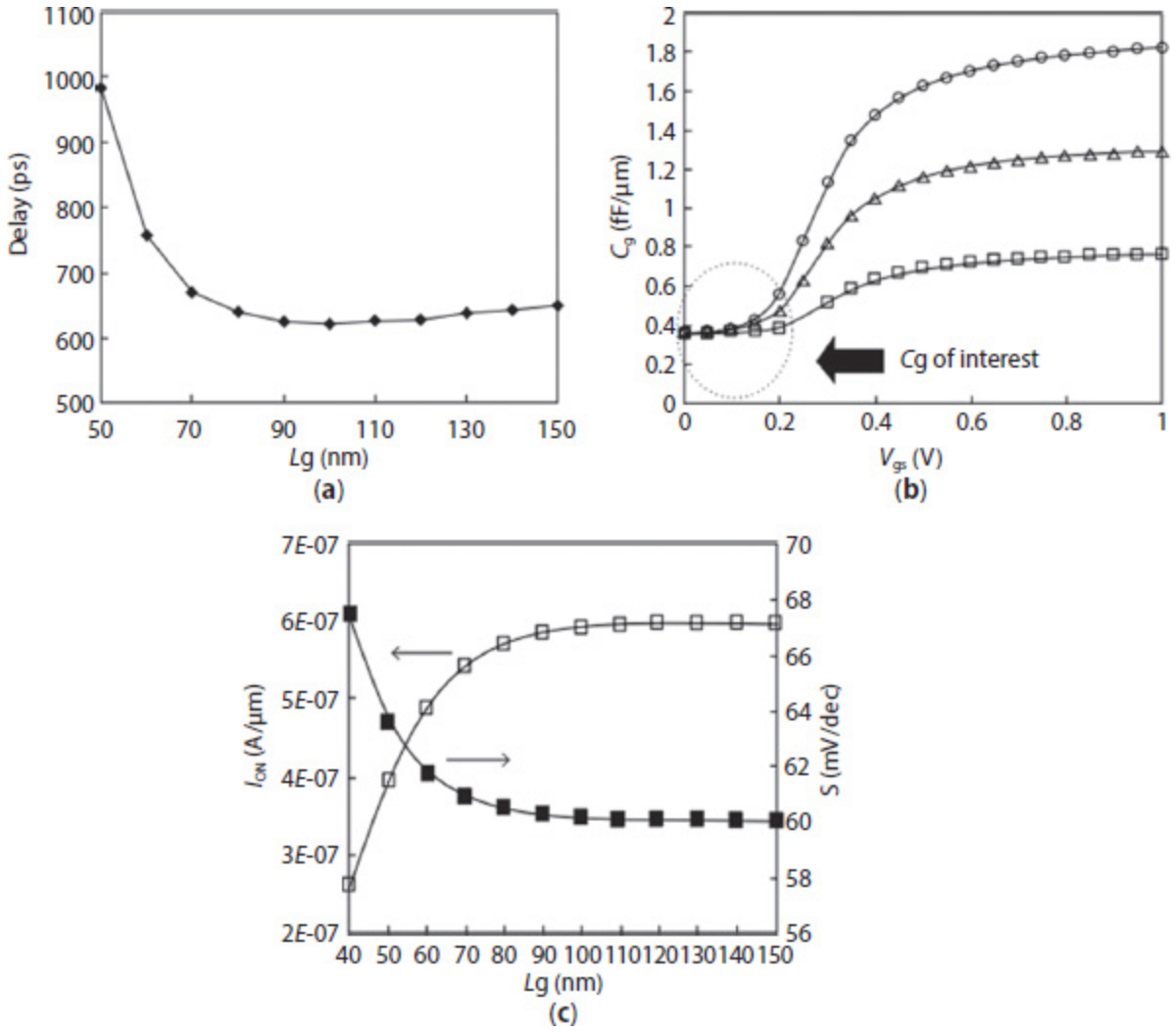

Figure 1.8 (a) Delay vs gate length of an inverter (b) Gate capacitance vs gate voltage of a DG n-channel MOSFET and (c) ON current and subthreshold slope vs gate length [65].

It is reported that properly optimized multi-gate devices can improve the performance of delay, power delay product, gate capacitance, energy consumption, and range of frequency significantly in subthreshold regions. In addition, if a suitable Codesign methodology is developed at the device, circuit, and architecture level for multi-gate devices operating in a sub-threshold regime, the above-mentioned performances can be improved even more [66]. Thus, it shows that properly optimized multi-gate gate devices are more suitable for subthreshold transistors as they have more control over current conduction, lesser gate capacitance, and therefore, better performance.

Device structures and materials, such as DGSOI, carbon nanotube, gate-all-around transistors, SOI-MOSFETs, FinFETs, and stacked transistors, have low power consumption, better performance and scalability, and excellent channel electrostatics and subthreshold swing compared to planar bulk MOSFETs [67]. FinFETs have been used successfully up to a 7-nm node due to their thin body and enhanced gate control on the channel from three sides [68–70]. It is also reported that the multi-fin FinFET structure has better trans-conductance and current drive by increasing the effective channel width by increasing the number of fins [71]. The nanosheet transistors have better gate control compared with FinFETs and therefore, less short channel effects, which are more suitable for logic applications. The single-stack Nanosheet with three vertically stacked channels has larger effective channel width compared to multi-fin FinFET transistors and therefore, better performance for the same footprint dimension [72, 73]. Therefore, if these structures with proper optimization are used for sub-threshold transistors, better performance can be expected. However, very few applications of these structures have been reported for subthreshold transistors [74–78].

Recently, the use of the negative capacitance effect in transistors for increasing the effective gate capacitance and improving gate control over the channel and subthreshold slope without changing the device structure is reported [79–84].

The negative capacitance phenomenon is an old concept but its application in semiconductor devices, particularly in MOSFET and TFET, is new.

To incorporate the negative capacitance effect in the devices, a layer of Ferroelectric materials such as SBT (strontium bismuth tantalite) is included with the gate stack of the reference MOSFET or other devices. Normally, in Ferroelectric materials, the electrons occupy the states in the lowest energy valley (e.g., at P in Figure 1.9a), but upon proper voltage application the band structure changes and the barrier reduces, causing an electron to pass through the middle region where it shows negative capacitance. If it is done with MOSFET, an MFMIS-type structure is formed, so the total gate capacitance (C) of the device becomes a series combination of capacitance due to the FE layer (C_{FE}) and reference device gate capacitance (C_{ox}), as expressed below:

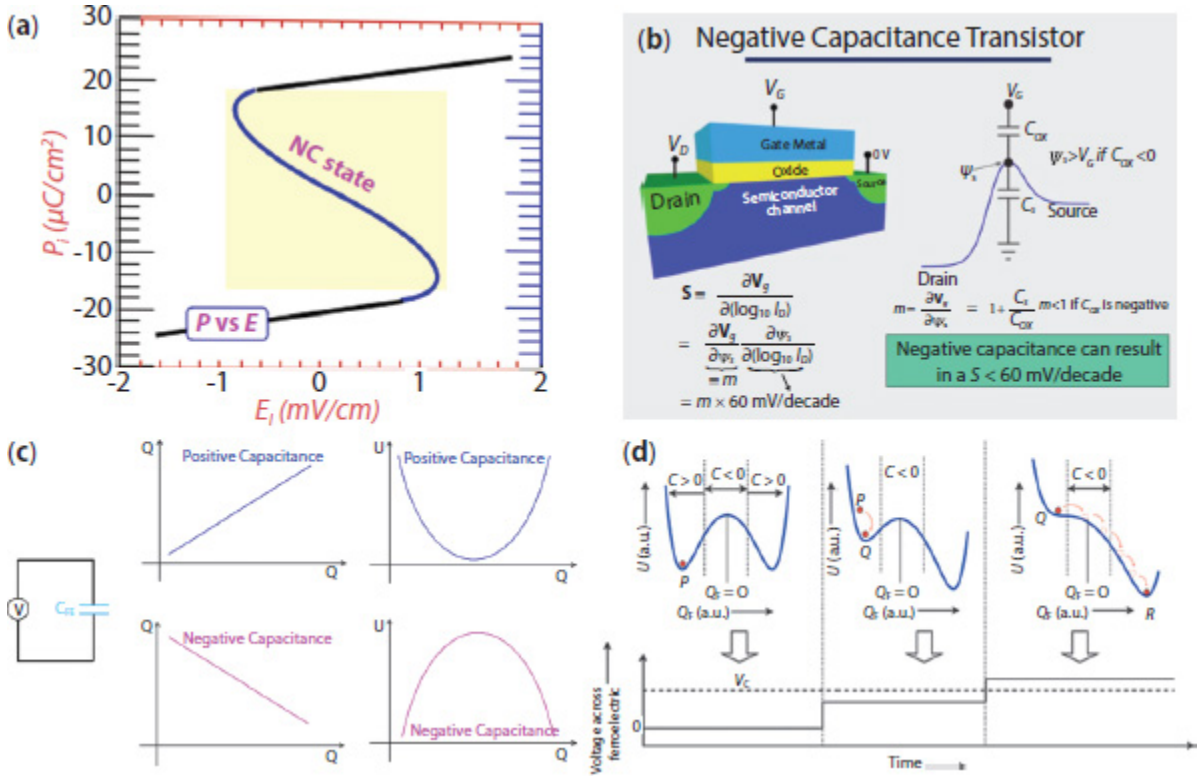

Figure 1.9 (a) Polarization in FE materials; (b) NC in MOSFETs; (c) charge voltage and energy vs. charge in positive and negative capacitances; (d) negative capacitance in FE materials vs. voltage [67].

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{FE}}$$

Total capacitance decides the hysteric or non-hysteric regions of the operation of the device. For the non-hysteric regions, it should be positive [67]. Since the hysteric region of operation has instability issues and the non-hysteric region does not, the latter is preferred over the former in device operation. Also, the non-hysteric region of operation provides significant improvement in the figure of merits of the device along with stability in output. For achieving maximum C, the negative capacitance of the FE layer should be nearly equal to the gate capacitance of the reference device. In other words, it limits the thickness of the FE layer that can be used in the gate stack without changing the polarization from non-hysteric to hysteric regions. The next step is calculating the shift in gate voltage due to the negative capacitance effect of the FE layer, following the 1D Landau-Khalantnikov (L-K) model [83, 84]:

$$V_G - V_{G,eff} = 2\alpha t_{fe} Q_{fe} + 4\beta t_{fe} Q_{fe}^3 + 6\gamma t_{fe} Q_{fe}^5$$

where α, β, and γ are Landau coefficients for SBT and equal to -1.3x10^8 m/F, 1.3x10^{10} m^5 /F/C^2, and 0m^9 /F/C^4, respectively [67]. The process of obtaining effective gate voltage, V_G, as a result of shifting due to different FE layer thicknesses, t_{fe}, is like that given in [67]. The equation shows the shift in the gate voltage due to NC. It implies that the same current can be obtained at a lower gate voltage or that the current has been increased for the same gate voltage compared to non-NC conditions. Therefore, the NC effect enhances the current and reduces the subthreshold slope, as shown in Figure 1.10. So, the subthreshold performance can be enhanced by the NC effect without changing the structure of the device.

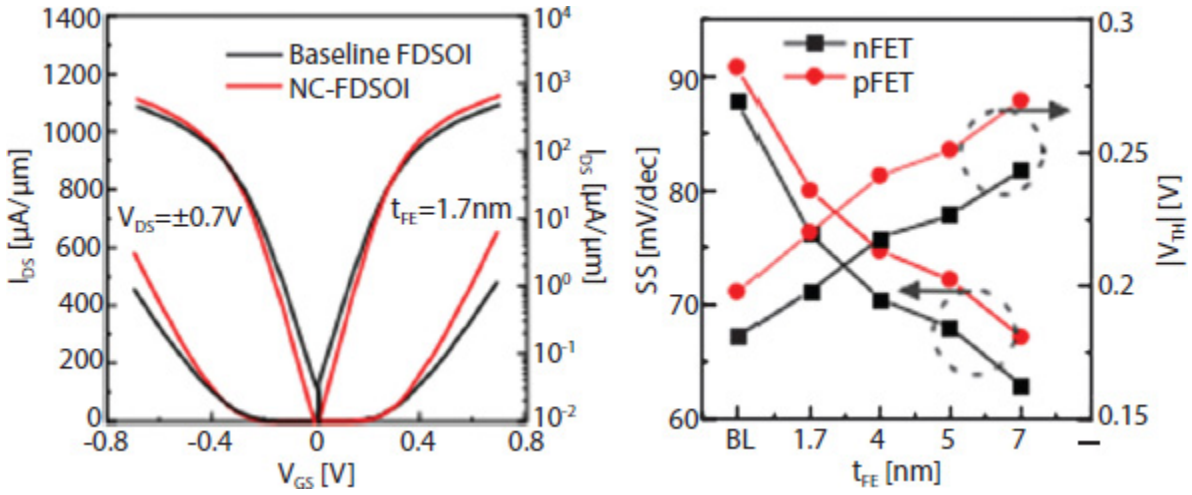

Figure 1.10 Impact of NC on current, subthreshold slope, and threshold voltage [82].

The comparison of conventional MOSFET and DGSOI is shown in Table 1.2. It clearly shows better performance from DGSOI over the bulk CMOS.

The feasibility of subthreshold transistors in digital applications, such as pseudo-N-MOS, variable threshold, domino, and pass transistors logics, is also encouraging [44, 86]. Due to higher voltage swing, ideal voltage transfer curve, robustness, less power consumption, and faster speeds, subthreshold pseudo-NMOS are more suitable compared to conventional pseudo-NMOS operating in the inversion region. To overcome the instability in device behavior because of temperature and process variations, variable threshold and dynamic threshold logics for subthreshold

regions have been proposed and are found to have encouraging results (see Table 1.3) [44, 86]. For accommodating higher frequency operations, domino logic in the subthreshold region is proposed and has shown encouraging results [84–88].

Table 1.2 Parameter comparison between Bulk CMOS and DGSOI at equal supply voltage and off current [85].

Parameter	**Bulk CMOS**	**DGSOI**
I_{ON} for standard device (A/m)	0.101	1.29
I_{ON} for optimized device (A/m)	0.162	1.93
PDP of an inverter with standard device (J)	5.5×10^{-16}	0.35×10^{-16}
PDP of a CMOS inverter with optimized device (J)	2.8×10^{-16} (48% better than standard)	0.30×10^{-16} (17% better than standard)
PDP of a Sub-Pseudo-NMOS inverter with optimized device (J)	2.2×10^{-16}	0.25×10^{-16}
Power-throughput tradeoff by device/circuit and architecture Codesign compared to conventional design	2.5 × improvement	3.8 × improvement

Table 1.3 Impact of parameters variation in strong inversion and sub-threshold operations [44, 86].

Parameter	Strong inversion-CMOS	Sub-CMOS	VT-Sub-CMOS
V_{th} variations (± 10%)	0.1–1.4%	34.7–96.2%	5–42.4%
Temperature variations (25−10°C)	28.2%	61.5%	33.7%

Parameter	Sub-CMOS	Subdomino
Power (nw)	10.64	3.408 (32%)
Delay (μs)	7.545	2.423 (3× faster)
PDP (fJ)	80.28	8.26 (10%)
Area (μm^2)	2381	1447 (60%)
Noise margins	poor	excellent

1.4 Conclusions

With continuous downscaling of device size as well as supply voltage, sub-threshold transistors have a very bright future in low and ultra-low-power applications. The continuous research in the area has shown that multigate devices, FinFETs, and CNTFETs can be used in subthreshold regions. In addition, by incorporating the negative capacitance effect, these devices have become even more attractive for subthreshold operations due to enhanced gate control over current conduction. Similarly, for logic design, pseudo-N-MOS, variable threshold, domino, and pass transistors can be suitable choices for subthreshold applications as they are robust, fast, and consume less power.

References

1. A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, “Low power CMOS digital design,” *IEEE Journal of Solid-StateCircuits*, vol. 27, no. 4, pp. 473–484, 1992.

2. B. C. Paul, H. Soeleman, and K. Roy, “An 8 × 8 subthreshold digital CMOS carry save array multiplier,” in *Proceedings of the 27th European Solid-State Circuits Conference (ESSCIRC ’01)*, pp. 377–380, Villach, Austria, September 2001.

3. C. H.-I. Kim, H. Soeleman, and K. Roy, “Ultra-low-power DLMS adaptive filter for hearing aid applications,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 11, no. 6, pp. 1058–1067, 2003.

4. A. Wang and A. P. Chandrakasan, “A 180mV FFT processor using subthreshold circuit techniques,” in *Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC ’04)*, vol. 1, pp. 292–529, San Francisco, Calif, USA, February 2004.

5. A. Wang and A. P. Chandrakasan, “A 180-mV subthreshold FFT processor using a minimum energy design methodology,” *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 310–319, 2005.

6. B. Zhai, L. Nazhandali, J. Olson, *et al.*, “A 2.60pJ/inst subthreshold sensor processor for optimal energy efficiency,” in *Proceedings of the IEEE Symposium on VLSI Circuits (VLSIC ’06)*, pp. 154–155, Honolulu, Hawaii, USA, June 2006.

7. B. H. Calhoun, A. Wang, N. Verma, and A. P. Chandrakasan,“Subthreshold design: the challenges of minimizing circuit energy,” in *Proceedings of the 11th ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED ’06)*, pp. 366–368, Tegernsee, Germany, October 2006.

8. Roy, K., Mukhopadhyay, S. and Mahmoodi-Meimand, H., 2003. Leakage current mechanisms and leakage reduction techniques in deep-submicrometric CMOS circuits. *Proceedings of the IEEE*, *91*(2), pp.305-327.

9. R. Pierret, *Semiconductor Device Fundamentals*. Reading, MA: Addison-Wesley, 1996, ch. 6, pp. 235–300.

10. Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. New York: Cambridge Univ. Press, 1998, ch. 2, pp. 94–95.

11. J. M. Rabaey, *Digital Integrated Circuits*. Englewood Cliffs, NJ: Prentice-Hall, 1996, ch. 2, pp. 55–56.

12. Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. New York: Cambridge Univ. Press, 1998, ch. 3, pp.143–144.

13. R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous,and A. R. LeBlanc, "Design of ion-implanted MOSFETs with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. SC-9,p. 256, 1974.

14. V. De, Y. Ye, A. Keshavarzi, S. Narendra, J. Kao, D. Somasekhar, R. Nair, and S. Borkar, "Techniques for leakage power reduction, "in *Design of High-Performance Microprocessor Circuits*, A. Chandrakasan, W. Bowhill, and F. Fox, Eds. Piscataway, NJ: IEEE,2001, ch. 3, pp. 48–52.

15. S. Chung and C.-T Li, "An analytical threshold-voltage model oftrenchisolated MOS devices with nonuniformly doped substrates," *IEEE Trans. Electron Devices*, vol. 39, pp. 614–622, Mar. 1992.

16. BSIM Group. MOSFET Model. Univ. California, Berkeley. Online]. Available: http://www2.eecs.berkeley.edu/Pubs/TechRpts/1998/ERL-98-51.pdf

17. J. Mandelman and J. Alsmeir, "Anomalous narrow channel effect intrenchisolated burried channel P-Mosfets," *IEEE Electron Device Lett.*, vol. 15, pp. 496–498, Dec. 1994.

18. Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. New York: Cambridge Univ. Press, 1998, ch. 3, pp.140–143.

19. *Fundamentals of Modern VLSI Devices*. New York: Cambridge Univ. Press, 1998, ch. 2, pp. 95–97.

20. K. Schuegraf and C. Hu, "Hole injection Sio2 breakdown model forvery low voltage lifetime extrapolation," *IEEE Trans. Electron Devices*, vol. 41, pp. 761– 767, May 1994.

21. Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. New York: Cambridge Univ. Press, 1998, ch. 2, pp. 97–99.

22. *Fundamentals of Modern VLSI Devices*. New York: Cambridge Univ. Press, 1998, ch. 2, pp. 99–100.

23. K. Roy and S. C. Prasad, *Low-Power CMOS VLSI Circuit Design*. New York: Wiley, 2000, ch. 2, pp. 28–29.

24. *Low-Power CMOS VLSI Circuit Design*. New York: Wiley, 2000, ch. 2, pp. 27–28.

25. K. Roy and S. C. Prasad, *Low-Power CMOS VLSI Circuit Design*. New York: Wiley, 2000, ch. 5, pp. 224–226.

26. S. Thompson, P. Packan, and M. Bohr, "MOS scaling: Transistor challenges for the 21st century," *Intel Technol. J.*, 3rd quarter 1998.

27. D. Fotty, *MOSFET Modeling with SPICE*. Englewood Cliffs, NJ: Prentice-Hall, 1997, ch. 11, pp. 396–397.

28. V. De, Y. Ye, A. Keshavarzi, S. Narendra, J. Kao, D. Somasekhar, R. Nair, and S. Borkar, "Techniques for leakage power reduction," in *Design of High-Performance Microprocessor Circuits*, A. Chandrakasan, W. Bowhill, and F. Fox, Eds. Piscataway, NJ: IEEE,2001, ch. 3, pp. 52–55.

29. Y. Ye, S. Borkar, and V. De, "New technique for standby leakage reduction in high-performance circuits," in *Dig. Tech. Papers Symp. VLSI Circuits*, 1998, pp. 40–41.

30. Z. Chen, M. Johnson, L. Wei, and K. Roy, "Estimation of standby leakage power in CMOS circuits considering accurate modeling of transistor stacks," in *Proc. Int. Symp. Low Power Electronics and Design*, 1998, pp. 239–244.

31. M. C. Johnson, D. Somasekhar, and K. Roy, "Leakage control with efficient use of transistor stacks in single threshold CMOS," in *Proc. ACM/IEEE Design Automation Conf.*, 1999, pp. 442–445.

32. N. Sirisantana, L. Wei, and K. Roy, "High-performance low-power CMOS circuits using multiple channel length and multiple oxide thickness," in *Proc. Int. Conf. Computer Design*, 2000, pp. 227–232.

33. Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. New York: Cambridge Univ. Press, 1998, ch. 4, p. 194.

34. S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J.Yamada, "1-V power supply high-speed digital circuit technology with multi-threshold voltage CMOS," *IEEE J. Solid-State Circuits,* vol. 30, pp. 847–854, Aug. 1995.

35. S. Shigematsu, S. Mutoh, Y. Matsuya, Y. Tanabe, and J. Yamada, "A1-V high speed MTCMOS circuit scheme for power-down applications," *IEEE J. Solid-State Circuits,* vol. 32, pp. 861–869, June 1997.

36. L. Wei, Z. Chen, M. Johnson, K. Roy, Y. Ye, and V. De, "Design and optimization of dual threshold circuits for low voltage low power applications," *IEEE Trans. VLSI Systems*, pp. 16–24, Mar. 1999.

37. P. Pant, V. K. De, and A. Chatterjee, "Simultaneous power supply, threshold voltage, and transistor size optimization for low-power operation of CMOS circuits," *IEEE Trans. VLSI Syst.*, vol. 6, pp.538–545, Dec. 1998.

38. A. J. Bhavnagarwala, B. L. Austin, K. A. Bowman, and J. D.Meindl, "A minimum total power methodology for projecting limits on CMOS GSI," *IEEE Trans. VLSI Syst.*, vol. 8, pp. 235–251, June2000.

39. S. Tyagi*et al.*, "A 130 nm generation logic technology featuring70 nm transistors, dual Vt transistors and 6 layers of Cu interconnects," in *Dig. Tech. Papers Int. Electron Devices Meeting*, 2000,pp. 567–570.

40. M. Takahashi *et al.*, "A 60-mw MPEG4 video codec using cluster voltage scaling with the variable supply-voltage scheme," *IEEE J. SolidState Circuits*, vol. 33, pp. 1772–1780, Nov. 1998.

41. T. D. Burd, T. A. Pering, A. J. Stratakos, and R. W. Brodersen, "A dynamic voltage scaled microprocessor system," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1571–1580, Nov. 2000.

42. H. Soeleman and K. Roy, "Ultra-low power digital subthreshold logic circuits," in *Proceedings of the International Symposium on Low Power*

Electronics and Design (ISLPED ’99),pp. 94–96, San Diego, Calif, USA, August 1999.

43. H. Soeleman, K. Roy, and B. C. Paul, “Robust subthreshold logic for ultra-low power operation,” *IEEE Transactions on very Large Scale Integration (VLSI) Systems*, vol. 9, no. 1, pp.90–99, 2001.

44. H. Soeleman, K. Roy, and B. C. Paul, “Robust ultra-low-power subthreshold DTMOS logic,” in *Proceedings of the International Symposium on Low Power Electronics and Design(ISLPED ’00)*, pp. 25–30, Rapallo, Italy, July 2000.

45. O. C. Akgun and Y. Leblebici, “Weak inversion performance of CMOS and DCVSPG logic families in sub-300 mV range,” in *Proceedings of the IEEE International Symposium on Circuitsand Systems (ISCAS ’06)*, pp. 1251–1254, Island of Kos, Greece,May 2006.

46. V. Moalemi and A. Afzali-Kusha, “Subthreshold pass transistor logic for ultra-low power operation,” in *Proceedings of the IEEE computer Society Annual Symposium on VLSI (ISVLSI ’07)*, pp.490–491, Porto Alegre, Brazil, March 2007.

47. B. H. Calhoun, A. Wang, and A. P. Chandrakasan, “Devicesizing for minimum energy operation in subthreshold circuits,” in *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC ’04)*, pp. 95–98, San Jose, Calif, USA, October 2004.

48. B. H. Calhoun, A. Wang, and A. P. Chandrakasan, “Modeling and sizing for minimum energy operation in subthreshold circuits,” *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp.1778–1786, 2005.

49. Y. K. Ramadass and A. P. Chandrakasan, “Minimum energy tracking loop with embedded DC-DC converter enabling ultra-low-voltage operation down to 250 mV in 65 nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 43, no. 1, pp. 256–265, 2008.

50. B. H. Calhoun, *Low energy digital circuit design using subthreshold operation*, Ph.D. thesis, Electrical and Computer Engineering Department, MIT, Cambridge, Mass, USA, December 2005.

51. A. Wang, *An ultra-low voltage FFT processor using energy-aware techniques*, Ph.D. thesis, Electrical and Computer engineering department, MIT, Cambridge, Mass, USA, February 2004.

52. B. C. Paul and K. Roy, “Oxide thickness optimization for digital subthreshold operation,” *IEEE Transactions on Electron Devices*, vol. 55, no. 2, pp. 685–688, 2008.

53. J.-J. Kim and K. Roy, “Double gate-MOSFET subthreshold circuit for ultralow-power applications,” *IEEE Transactions on Electron Devices*, vol. 51, no. 9, pp. 1468–1474, 2004.

54. B. C. Paul, A. Bansal, and K. Roy, “Underlap DGMOS for digital-subthreshold operation,” *IEEE Transactions on Electron Devices*, vol. 53, no. 4, pp. 910– 913, 2006.

55. P.K. Asthana, B.Ghosh, Y. Goswami, and B.M.M.Tripathi, 2014. High-speed and low-power ultradeep-submicrometer III-V heterojunctions tunnel field-effect transistor. *IEEE Transactions on Electron Devices*, *61*(2), pp.479-486.

56. P. Bal, B.Ghosh, P.Mondal, M.W.Akram, and B.M.M.Tripathi, 2014. Dual material gate junctionless tunnel field effect transistor. *Journal of Computational Electronics*, *13*(1), pp.230-234.

57. B.M.M.Tripathi, P.Jain, and S.P.Das, 2017. SiGe Source Dual Metal Double Gate Tunnel Field Effect Transistor. *Journal of Low Power Electronics*, *13*(1), pp.76-82.

58. S.B.Rahi, S.Tayal, and A.K.Upadhyay, (2021). A review on emerging negative capacitance field effect transistor for low power electronics. *Microelectronics Journal*, *116*, 105242.

59. S.B. Rahi, and B.Ghosh. “High-k double gate junctionless tunnel FET with a tunable bandgap.” *RSC Advances* 5, no. 67 (2015): 54544-54550.

60. M.Sathish Kumar, T.S. A. Samuel, K. Ramkumar, I. V.Anand, and S. B. Rahi. “Performance evaluation of gate engineered InAs–Si heterojunction surrounding gate TFET.” *Superlattices and Microstructures* 162 (2022): 107099.

61. N.Guenifi, S. B. Rahi, and M. Larbi. “Suppression of Ambipolar current and analysis of RF performance in double gate tunneling field effect transistors for low-power applications.” *Int J nanoparticles nanotech* 6 (2020): 033.

62. Naima, Guenifi, and S.B. Rahi. “Low power circuit and system design hierarchy and thermal reliability of tunnel field effect transistor.” *Silicon* 14, no. 7 (2022): 3233-3243.

63. S.Tayal, S.B. Rahi, J.P.Srivastava, & S. Bhattacharya, (2021). Recent Trends in Compact Modeling of Negative Capacitance Field-Effect Transistors. In *Semiconductor Devices and Technologies for Future Ultra Low Power Electronics* (pp. 203-226). CRC Press.

64. S.Tayal, A.K. Upadhyay, D.Kumar, & S.B.Rahi, (Eds.). (2022). *Emerging Low-Power Semiconductor Devices: Applications for Future Technology Nodes*. CRC Press. 65].

65. J.-J. Kim and K. Roy, “Double gate-MOSFET subthreshold circuit for ultralow-power applications,” *IEEE Transactions on Electron Devices*, vol. 51, no. 9, pp. 1468–1474, 2004.

66. [13]J.-J. Kim and K. Roy, “Double gate-MOSFET subthreshold circuit for ultralow-power applications,” *IEEE Transactions on Electron Devices*, vol. 51, no. 9, pp. 1468–1474, 2004.

67. J.P.Colinge, ed., 2008. *FinFETs and other multi-gate transistors* (Vol. 73). New York: Springer.

68. K.Cheng, C.Park,, C.Yeung, *et al.*, 2016, December. Air spacer for 10nm FinFET CMOS and beyond. In *2016 IEEE International Electron Devices Meeting (IEDM)* (pp. 17-1).

69. J. Singh, J. Ciavatti, *et al.*, 2017. 14-nm FinFET technology for analog and RF applications. *IEEE Transactions on electron devices*, *65*(1), pp.31-37.

70. C. W. Yeung*et al.*, “Channel geometry impact and narrow sheet effect of stacked nanosheet,” in *IEDM Tech. Dig.*, Dec. 2018, pp. 28.6.1–28.6.4.

71. T. B. Hook, “Power and technology scaling into the 5 nm node with stacked nanosheets,” *Joule*, vol. 2, no. 1, pp. 1–4, Jan. 2018.

72. P. Feng and P. Ghosh, “Design consideration in the development of multi-fin FETs for RF applications,” *World J. Nano Sci. Eng.*, vol. 2, no. 2, pp. 88–91, 2012.

73. W. Wu and M. Chan, “Analysis of geometry-dependent parasitics in multifin double-gate FinFETs,” *IEEE Trans. Electron Devices*, vol. 54, no. 4, pp. 692–698, Apr. 2007.

74. N. Loubet*et al.*, “Stacked nanosheet gate-all-around transistor to enablescaling beyond FinFET,” in *IEEE Symp. VLSI Technol. Dig. Tech.Papers*, Jun. 2017, pp. T230–T231.

75. J. Zhang *et al.*, “High-k metal gate fundamental learning and multi-Vtoptions for stacked nanosheet gate-all-around transistor,” in *IEDM Tech.Dig.*, Dec. 2017, pp. 22.1.1–22.1.4.

76. S. Barraud*et al.*, “Performance and design considerations for gateall-around stacked-NanoWires FETs,” in *IEDM Tech. Dig.*, Dec. 2017,pp. 29.2.1–29.2.4.

77. D. Yakimets*et al.*, “Power aware FinFET and lateral nanosheet FETtargeting for 3 nm CMOS technology,” in *IEDM Tech. Dig.*, Dec. 2017,pp. 20.4.1–20.4.4.

78. D. Jang *et al.*, “Device exploration of NanoSheet transistors for sub-7-nm technology node,” *IEEE Trans. Electron* Devices, vol. 64, no. 6,pp. 2707–2713, Jun. 2017.

79. S.Salahuddin and S.Datta, “Use of negative capacitance to provide voltage amplification for low power nanoscale devices,” *Nano Lett.*,vol. 8, no. 2, pp. 405–410, 2008.

80. B.M.M. Tripathi and S.P.Das, 2019. Analysis of Parameter Variations and Their Impact on Hetero-Junctionless Tunnel Field Effect Transistor Due to Negative Capacitance. *Advanced Science, Engineering and Medicine*, *11*(8), pp.728-733.

81. A. K. Upadhyay, S. B. Rahi, S. Tayal, Y. S. Song, Recent progress on negative capacitance tunnel FET for low-power applications: Device perspective, Microelectronics Journal, 2022, 105583, ISSN 0026-2692.

82. O.Prakash., A.Gupta, G.Pahwa, Y.S.Chauhan, and H.Amrouch, 2021. On the Critical Role of Ferroelectric Thickness for Negative Capacitance Device-Circuit Interaction. *IEEE Journal of the Electron Devices Society*, *9*, pp.1262-1268.

83. G. A. Salvatore, D. Bouvet, A. M. Ionescu. In *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, 1–4. IEEE, (2008).

84. A. Starkov, I. Starkov. *Ferroelectrics*, 461, 50–60, (2014).

85. A. Raychowdhury, B. C. Paul, S. Bhunia, and K. Roy, "Ultralow power computing with subthreshold leakage: a comparative study of bulk and SOI technologies," in *Proceedings of the Conference on Design, Automation and Test in Europe (DATE '06)*, vol. 1, pp. 856–861, Munich, Germany, 2006.

86. H. Soeleman, K. Roy, and B. C. Paul, "Sub-domino logic: ultra-low power dynamic subthreshold digital logic," in *Proceedings of the 14th International Conference on VLSI Design (VLSI DESIGN '01)*, pp. 211–214, Bangalore, India, January 2001.

87. O. C. Akgun and Y. Leblebici, "Weak inversion performance of CMOS and DCVSPG logic families in sub-300 mV range, "in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS '06)*, pp. 1251–1254, Island of Kos, Greece, May 2006.

88. V. Moalemi and A. Afzali-Kusha, "Subthreshold pass transistor logic for ultra-low power operation," in *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI '07)*, pp. 490–491, Porto Alegre, Brazil, March 2007.

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2
Introduction to Conventional MOSFET and Advanced Transistor TFET

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Abstract

Integrated circuits have undergone significant development over the past several decades. Because of the increased density of transistors in CMOS devices, faster, more efficient, and more complex electronics are all feasible. Since more people are using mobile devices, it is crucial that digital and analogue circuits are energy effective. MOSFETs and Fin-FETS cannot be reduced in their power consumption. At ambient temperature, the SS of thermionic transistors cannot be greater than 60 mV/dec. Alternative carrier injection devices without the Boltzmann distribution of mobile charge carriers owing to temperature are needed to overcome the SS limit of traditional transistors. Traditional field-effect transistors (FETs) have been a ubiquitous electronic component for quite some time. However, nanoelectronic systems based on FETs are inefficient due to their high switching voltage needs. Due to the subthreshold swing (SS) limitation, the supply voltage of typical FETs cannot be decreased by more than 60 mV/decade. To circumvent this issue, engineers created tunnel FETs

(TFETs). The most promising post-CMOS device is the Tunnel Field-Effect Transistor, which injects carriers without heat using the Band-To-Band Tunnelling (BTBT) effect. TFETs are “steep slope devices” since their slope is less than 60 mV/dec at room temperature. They are suitable for low-power, high-efficiency circuits. TFETs have developed most in digital circuits and applications.

***Keywords*:** MOSFET, Tunnel FET (TFET), quantum tunneling, subthreshold swing, Band-To-Band Tunnelling (BTBT), ultra-low power

2.1 Introduction

Tunnel field effect transistors (TFETs) could potentially replace field effect transistors (FETs) made from metal oxide semiconductors (MOSFETs). Silicon (Si) based TFETs are the most desirable because Si is already well understood. On the other hand, large-bandgap Si has low ON-current (I_{ON}) due to its low band-to-band tunneling (BTBT) efficiency. A heterostructure approach is utilized to boost the I_{ON} of TFET. However, this heterostructure TFET is only helpful for n-channel TFETs (n-TFETs) with low I_{ON}. Regarding complimentary p-TFET, there is no solution. People are interested in TFET due to its minimal subthreshold swing (SS) and low OFF-current (I_{OFF}).

As MOSFETs become smaller, the power supply voltage should also decrease. This will reduce the quantity of power concentrated in a limited region. To maintain a high I_{ON} and a low I_{OFF}, SS must be decreased. This is now one of the most vital concerns in technology. In an experiment, the subthreshold swing of a TFET is 60 mV/dec. Current is generated in a standard MOSFET by thermal emission of carriers across a potential barrier. Maintaining an appropriate power consumption range for conventional MOSFETs at advanced technical nodes is one of the most challenging issues [1–4]. Tunnel field-effect transistors (TFETs), which conduct current differently than MOSFETs, are a potential substitute for MOSFETs due to their electrical characteristics. The ON-state current density of TFET is two orders of magnitude lower than that of a high-performance MOSFET. People are considering employing materials with narrower bandgaps and smaller effective masses to increase the ON-state

tunneling current's strength. The SS of MOSFET cannot be made less than 60 mV/dec at room temperature. The TFET uses BTBT as a source carrier injection method, whereas MOSFET uses thermal carrier injection. In the following parts, we will compare TFET and MOSFET in terms of their construction, operation, and transfer characteristics.

2.2 Device Structure

The device shapes of TFETs and MOSFETs are comparable because they both feature doped regions and a gated channel. In contrast to MOSFETs, TFETs have oppositely doped sources and drains, as shown in Figure 2.1.

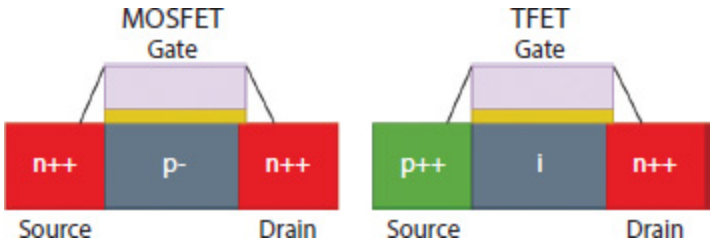

Figure 2.1 MOSFET and TFET doped region comparison.

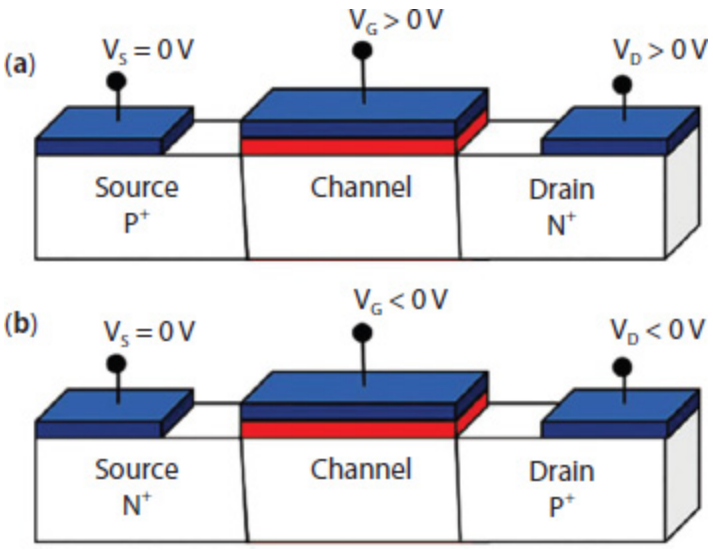

Figure 2.2 TFET biasing scheme: (a) n-type TFET and (b) p-type TFET.

For an n-type TFET, the source is at ground potential and the gate and drain are both driven by positive voltages. In order to create a p-type TFET, the source is tied to the ground while a negative voltage is applied to the drain and gate electrodes, as illustrated in Figure 2.2. When a TFET is activated,

an n-type or p-type carrier will predominate in the channel directly under the gate. If electrons are the predominant carrier in the channel, the TFET is said to be n-type. For a TFET to be classified as p-type, the channel must be dominated by holes.

2.3 TFET Principle of Operation

For a TFET to function, BTBT is essential. The basic structure is shown in Figure 2.3. To accomplish this, carriers in BTBT either cross the bandgap from the valence to the conduction band or vice versa.

2.3.1 OFF State

When $V_{DS} > 0$ and $V_{GS} = 0$, the TFET is in the OFF state just like a MOSFET. When a TFET is turned off, charged particles in the channel's conduction band tend to move toward the drain. This would result in a flow of current. However, because the source is a p-type, its conduction band contains extremely few free electrons. This indicates that just a small number of electrons can be injected into the channel. This significantly reduces the I_{OFF}. Remember that the source of a MOSFET is n-type and contains free electrons in that conduction band. A handful of these electrons will cross the potential barrier at the source-channel junction and enter the channel. This is known as thermionic emission. This makes the MOSFET's OFF-state current larger than that of the TFET [5]-[7].

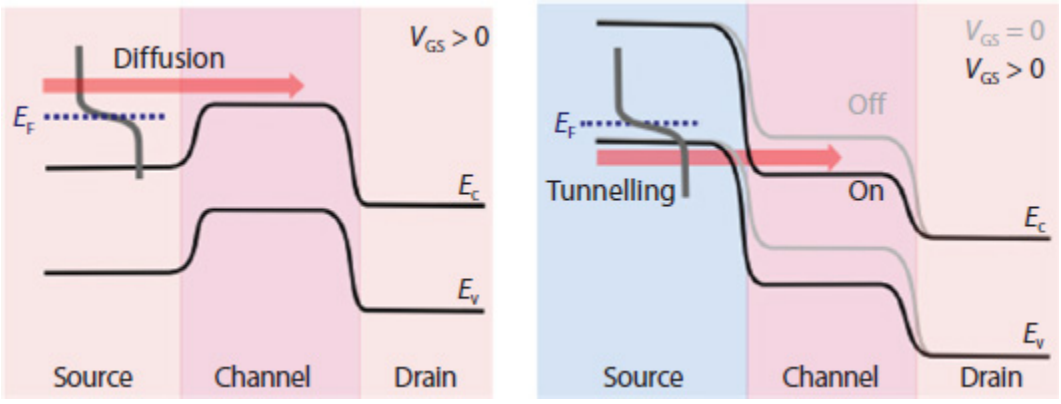

Figure 2.3 MOSFET and TFET schematic valence and conduction band diagrams.

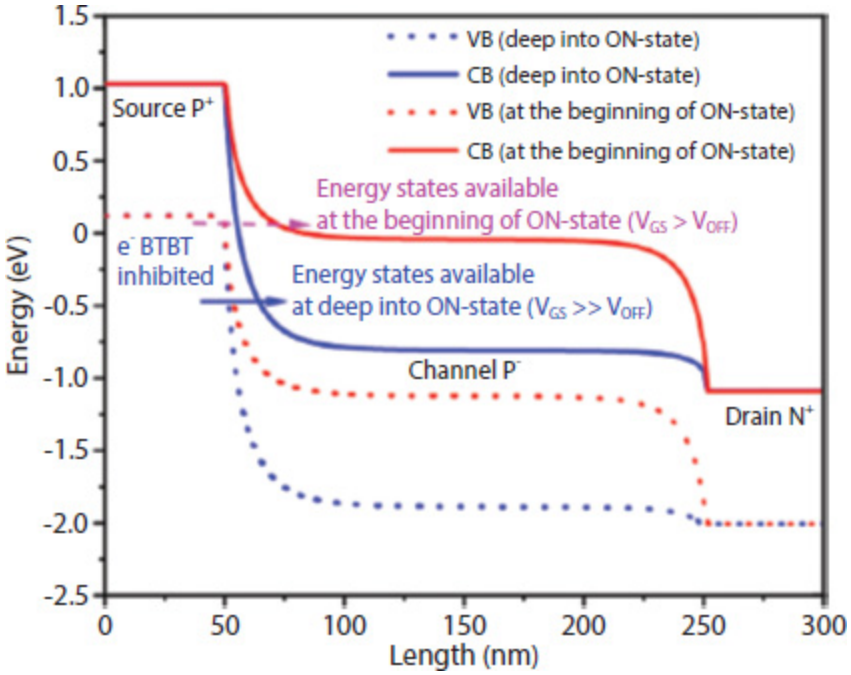

Figure 2.4 Band profile of TFET at beginning of and deep into ON state.

2.3.2 ON State

Energy bands in the channel shift in respect to the source if V_{GS} is increased. At a specific value of V_{GS}, the valence band of its source coincides with the conduction band of its channel. Figure 2.4 depicts the band profile of a TFET at the beginning and deep into the ON state.

The electrons in the source's valence band had no available energy state in the channel to tunnel into when the device was turned off. Electrons can tunnel from the source into the drain via the potential barrier created by the bandgap because the valence band of the source and the conduction band of the channel are in perfect alignment. The TFET's ON-state begins at V_{GS} where this alignment of the source valence band and the channel conduction band takes place.

2.4 Material Characterization

A TFET comprises of the P+ source, an intrinsic channel, and an n+ drain. Within the OFF state (V_G = 0V), the tunneling barrier is sufficiently strong to provide low I_{OFF} values [6]. When the gate voltage is present (V_G = 1V),

the band bending inside the intrinsic location decreases the barrier width, allowing electrons to tunnel from supply to channel. The overall schematic of a TFET and its band profile is shown in Figure 2.5.

Various potential solutions involving TFET materials are being considered to improve device performance.

2.4.1 Group IV Materials

Si is a popular material because it has few defects in bulk and at the gate dielectric interface and is easy to manufacture. There is a significant benefit from this. As Si is not an optimal BTBT material, most Si TFETs exhibit a mild I_{ON}. When the E_G is 1.12 eV, tunneling is highly improbable to occur. While I_{OFF} benefits from a slow tunneling rate, I_{ON} suffers.

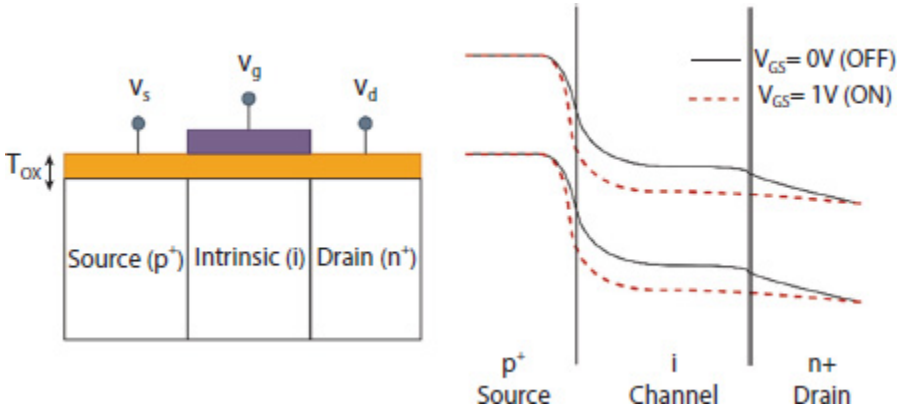

Figure 2.5 TFET schematic and energy band structure.

2.4.2 Group III-V Materials

More innovative technologies such as new channel material qualities that can deliver greater currents at the same voltage as Si FETs are required to lower the voltage level without sacrificing performance. The ON-current (I_{ON}) in nanoscale FETs is dependent on the injection velocity and the state density. In this sense, III-V materials like InAs and InGaAs make excellent n-channel MOSFET materials because they are able to create a big I_{ON} at a lower supply voltage than Si FETs if the electron injection speed is ideal and there are a sufficient number of electron states. In GaAs, MOSFETs have an injection speed that is more than twice as fast as Si MOSFETs, even at half the working voltage. Ge and III-V materials like GaSb, InSb,

and InGaSb show promise for p-channel MOSFETs and may enhance performance. Therefore, a second technology development will cause havoc in the application of high-mobility channel materials to silicon. It is necessary to increase the device's turn-on steepness in order to scale the voltage level lower (below 0.5 V) while maintaining high Ion and low OFF-current. This entails lowering a subthreshold swing below MOSFETs' 60-mV/decade limit and will necessitate a substantial modification to the machine's operation. Instead of thermally injecting free electrons into the channel, TFET uses quantum-mechanical band-to-band tunnelling (BTBT) in which charge carriers moving from one energy band to another. The most promising option for steep-slope switches right now is TFETs. They only require a supply voltage of about 0.3 V, which reduces power consumption significantly. III-V compound semiconductors and their heterostructures are required materials for this new innovation transition according to recent TFET performance data.

2.4.3 Heterostructures

So far, we've discussed different materials assuming that the device's active component is just one material. The correlation between I_{ON} and I_{OFF} is crucial when deciding the setup's material. You don't want I_{OFF} to increase as a result of I_{ON} improvement. Making a heterostructure out of two different materials that separate the materials in the source from the materials in the channel and drain is one way to separate the two. Heterostructures are either lattice-matched or lattice-mismatched, depending on the materials used.

2.4.4 2D Materials

We can utilize 2D materials in place of bulk semiconductors. Because of their exceptional gate control and thinness, 2D materials are gaining widespread attention. Even if there are no surface imperfections or loose bonds, it should still be able to achieve a low defect density. The most researched 2D material is graphene. It is a semimetal without a bandgap and is unsuitable for TFET. To create a bandgap, however, the symmetry must be broken either by stacking two layers of graphene and applying an electric field or by creating nanoribbons out of graphene. By adjusting the ribbon's size or the electric field's intensity, the bandgap can be fine-tuned.

2.5 Characteristics of TFET

2.5.1 Subthreshold Swing

TFETs are being considered as a replacement for MOSFETs due to their superior subthreshold swing (SS). Because TFETs operate via a tunneling mechanism, TFETs can have an SS lower than 60 mV/dec, which is the thermal limit for MOSFETs (i.e., thermionic injection).

SS for a MOSFET is given below:

$$SS = \left(\frac{d \log(I_{DS})}{dV_{GS}} \right) \tag{2.1}$$

Consequently, the SS and V_{GS} of a MOSFET are always identical. Instead, a TFET uses a “band-to-band tunneling” phenomenon to allow electrical current to flow even in the subthreshold zone. The tunneling rate is proportional to the electric field in the opposite direction.

In a TFET:

$$I_{DS} \, \alpha \, e^{-\frac{1}{E}} \tag{2.2}$$

Here, E is the lateral electric field as a function of V_{GS}. Therefore, unlike a MOSFET, the SS value in a TFET varies as a function of the gate voltage. TFET has two types of SS: point SS and average SS.

At a specific value of V_{GS}, the point SS is defined as

$$SS_{Point} = \left(\frac{dV_{GS}}{d\log(I_{DS})} \right) \tag{2.3}$$

Over a variety of V_{GS} values, the average SS is defined as

$$SS_{Avg} = \frac{(V_T - V_{OFF})}{\log(I_{VT}) - \log(I_{OFF})} \tag{2.4}$$

where Vth is the threshold voltage and V_{OFF} is the gate voltage in the OFF-state.

2.5.2 I_{ON}/I_{OFF} Ratio

The TFET is believed to be more appropriate for low electricity applications because of less leakage current (I_{OFF}). Additionally, gate-specific feature engineering achieves a fully low I_{OFF} and operating current (I_{ON}) in TFETs. Single Gate (S_G) SOI TFETs with a Silicon (Si) basis have the I_D - V_G feature, as shown in Figure 2.6. At constant drain bias, strong electron tunneling at the supply side causes the drain current (Id) to increase exponentially as gate voltage increases. The prospect for tunneling and I_{ON}'s relationship is as follows:

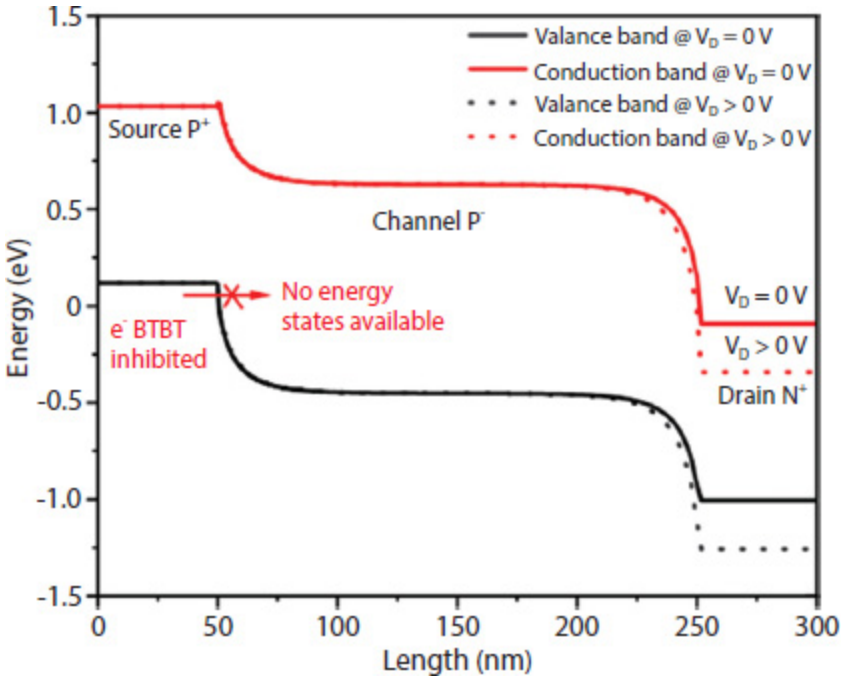

Figure 2.6 Band diagram along surface of TFET in OFF state (i.e., at V_{GS} = 0 V).

$$I_D \propto exp\left[-\frac{4\sqrt{m*E_g^{\frac{3}{2}}}}{3|e|h(E_g+)\Delta\varphi}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}t_{Si}t_{ox}}\right]\Delta\varphi \quad (2.5)$$

In the above equation, the band hole is Eg, the electron charge is e, the effective carrier mass is m, the electron charge is, and the capacity difference between the supply valence band and the channel conduction band is. The thicknesses of the oxide and silicon movies, respectively, are tox and tSi, in addition to the silicon and oxide dielectric constants. The equation, as mentioned above, clearly shows that lowering tox, raising ox, and lowering Eg would enhance tool performance [8, 9]. The Silicon Germanium on an Insulator (SGOI) TFET with a gate length (Lg) of 30 nm had a higher I_{ON}/I_{OFF} ratio [14]. Double fabric gate TFETs and p-n-i-n TFETs achieve higher I_{ON}/I_{OFF} ratios.

2.5.3 Ambipolar Effect

Because of the TFET's ambipolarity, a negative V_{GS} can cause a normally conducting nTFET to conduct like a usually conducting pTFET. As the electric field increases at the channel-drain junction, the n-type drain region is depleted. A hole tunneling current is injected into the channel after the valence band in the channel transitions to the conduction band in the drain. As the voltage gradient strengthens (V_{GS} decreases), the current strengthens. The behaviour can be good or bad depending on how it is used. The ambipolarity of a TFET can increase the switching leakage of a TFET inverter. Still, it can also be used to reduce the size of digital and analog circuits by allowing both positive and negative gate voltage switching to activate the tunneling current [10–12].

2.6 Comparison of OFF-State Characteristics

One of the main benefits of BTBT transistors is that they are able to reduce OFF-state leakage or standby energy dissipation in circuits. This is accomplished in devices by subthreshold functioning with SS below the typical limit. The device's temperature dependence features for the two designs are also compared (I_{DS}-V_{GS}). With SS = 60 mV/dec (at T = 300 K), the wrap-around gate's enhanced electrostatic control, shown in Figure 2.7, allows us to obtain the optimum subthreshold functionality. This will be well explained by observing the thermionic-emission process occurring within the OFF-current of a typical MOSFET [13].

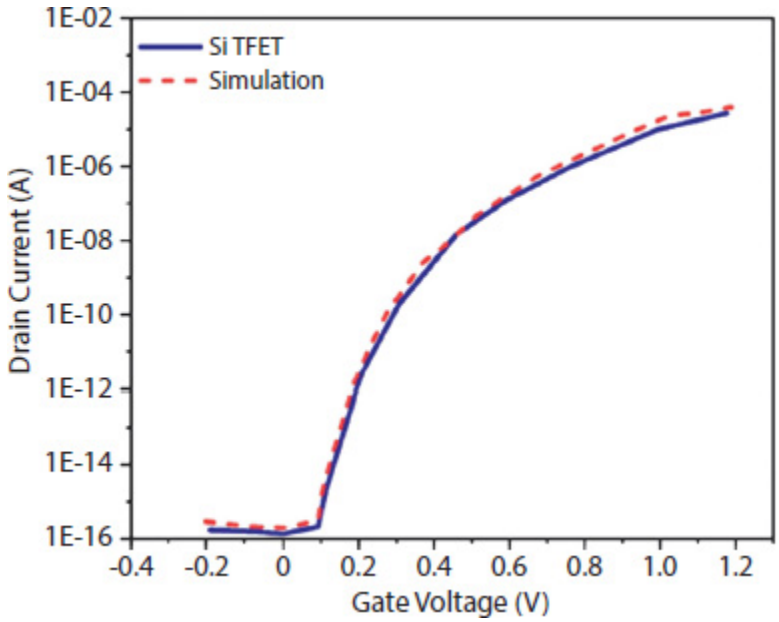

Figure 2.7 $I_D - V_G$ characteristics of single gate SOI-TFET.

Figure 2.8 illustrates that the OFF-current contemporary does not substantially degrade at high temperatures in ballistic transit. This occurs due to the domination bandgap in the supply area being closed by the thermal injection of excessive power. Because of the expansion of a Fermi distribution, there is a small rise in subthreshold modern at higher temperatures. A desirable aspect of TFETs that might assist in resolving the heat transfer issue is their capacity to produce off-level leakage currents that don't burn out at higher temperatures.

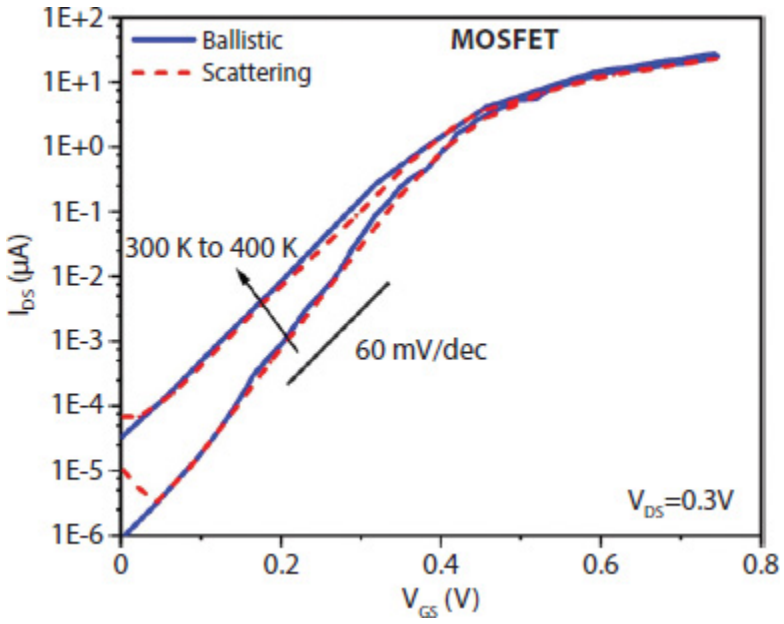

Figure 2.8 MOSFET I_{DS}-V_{GS} temperature correlation.

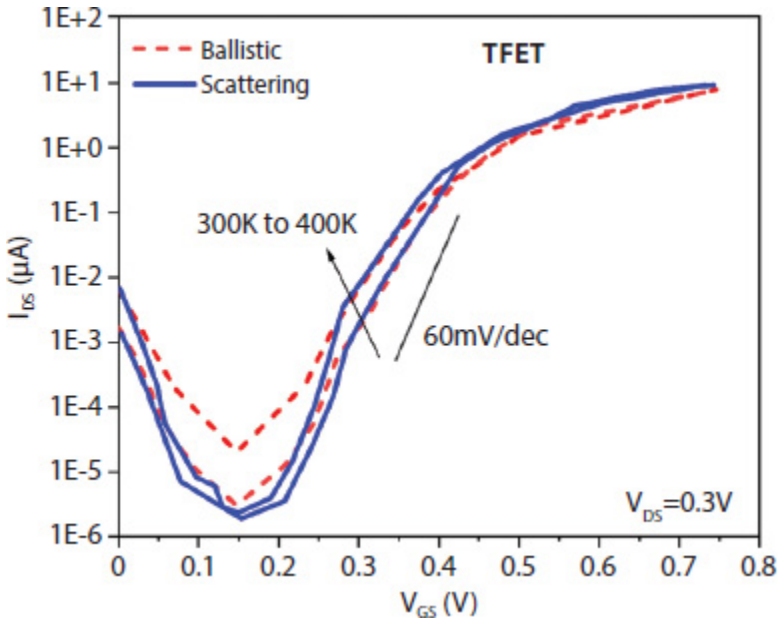

Figure 2.9 I_{DS}–V_{GS} dependence on temperature in TFET.

The I_{DS}-V_{GS} is perused to produce I_{OFF} and I_{ON} curves [13]. The ambipolar conduction seen in Figure 2.9 illustrates the increase in I_{OFF} observed in the TFET investigations at lower I_{ON} values (I_{ON} 0.6 A/tube). Compared to MOSFETs, TFETs show less IOFF deterioration during ballistic distribution at higher temperatures. Using the I_{OFF} versus I_{ON} temperature connection at

V_{DD} = 0, it is possible to see in how many device-biasing situations the TFET surpasses the MOSFET. It is well known in this region that the former has a lower I_{OFF} (and hence a lower Ps_{tandby}) at a positive I_{ON}. Thus, TFETs may be more suitable for low-energy systems with small drive-area needs.

2.7 Phonon Scattering's Impact

By using the thermionic-emission problem of modern conduction, we can observe that the MOSFET's subthreshold features are unaffected by phonon scattering. However, solid tunneling facilitated by phonons considerably enhances the initial phase of ambipolar conduction [14]. At low gate voltages, the BTBT found in carbon nano-tube (CNT) MOSFETs is more significant. It has been demonstrated that even when SS 60 mV/dec is maintained, SS decreases in the presence of phonon scattering in the TFET. Phonon-absorption-assisted distribution executes a full-size component within the deterioration under non-state-biasing circumstances. The sub-threshold cutting-edge is more strongly temperature-established because higher temperatures have enhanced phonon occupancy, which supports phonon-assisted distribution.

At V_{DD} = 3.0 V below dissipative transport, it may be demonstrated that the TFET still outperforms the MOSFET in the capacity biasing zone. The OFF-current leakage that is almost an order of magnitude is substantially less than the MOSFET and may still be reached at both room temperature and severe temperatures. When comparing the I_{OFF} to I_{ON} merely based on ballistic and dissipative shipping, it is evident that the ballistic approximation represents the advantages of TFET.

2.8 ON-State Performance Comparison

The ability of BTBT-based transistors to produce enough ON currents has been a significant problem. p-i-n TFETs have been used to improve the ON current. The issue persists even though several optimization methodologies for TFETs have been developed to improve I_{ON}. The characteristics of I_{DS}-V_{GS} for the two devices are compared in Figure 2.9 on a linear scale.

Compared to the MOSFET, the TFET's driven current is three times less. The I_{ON} degrades by a factor of 18 more than the MOSFET.

2.9 Performance Analysis Based on Intrinsic Delay

Intrinsic delay (τ), a crucial performance measure, demonstrates the inherent restrictions on switching frequency and AC parameters. Therefore, it considers any greater rate caused by the effects of edge capacitance. Figure 2.8 compares I_{ON}/I_{OFF} in reference to the TFET and MOSFET. When the I_{ON}/I_{OFF} ratio exceeds 10^4, the TFET is much quicker. A TFET's ON-OFF transition requires a significantly lower rate than a MOSFET's, which is the leading cause of this occurrence [15, 16]. The device delay for TFETs will increase dramatically because of the drop in I_{ON}. Additionally, phonon dispersion may be seen to enhance (τ) for each device. Figure 2.9 shows that even while the deterioration is noticeably worse when phonon scattering is present, the use of current TFETs is no longer severely reduced. The intrinsic device delay, as shown in Figure 2.10, is the same for the two devices. Still, a load capacitance, such as a lengthy link, might make the TFET substantially slower.

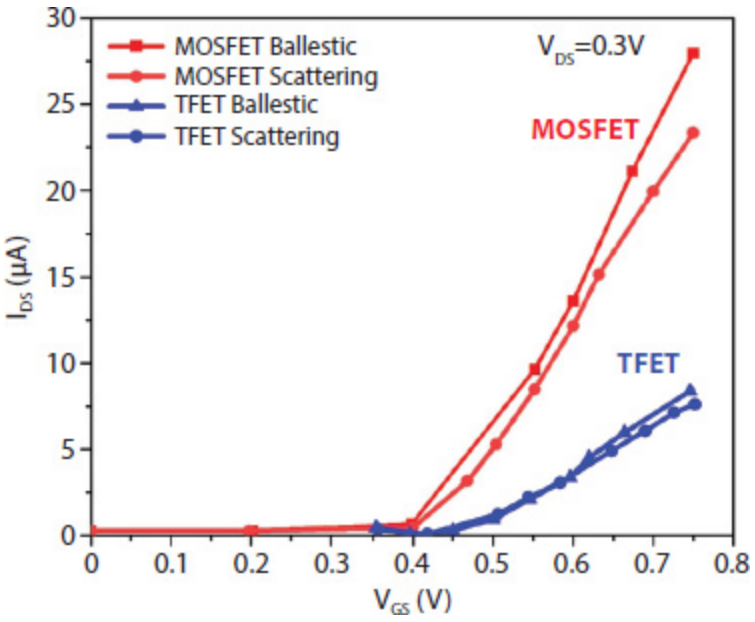

Figure 2.10 Comparison of MOSFET and TFET's linear IDS-VGS under dissipative and ballistic transport.

2.10 Bandgap's Effect on Device Performance

It's important to mention that the semiconductor bandgap affects typical performance metrics and device functioning. The following discussion may also have significant ramifications for nanowire and ultrathin-body semiconductor TFET devices where quantum confinement increases the digital bandgap. Since these systems enable more gate manipulation and the reduction of short-channel effects, they are definitely candidates for TFET devices. Between the Fermi supply (EFS) degree and the elevation of the channel conduction band, every tool has a constant injection barrier at V_{GS} = 0V after changing the characteristic of the gate metal. For substances with shorter bandgaps, in the ON state current [17] TFET performs better than the MOSFET when there is CNT tool biasing (Figures 2.11 and 2.12). The TFET is an intriguing example of a device that, despite today's increased electricity, lacks these kinds of benefits. The tool's high OFF state current leakage is the source of that.

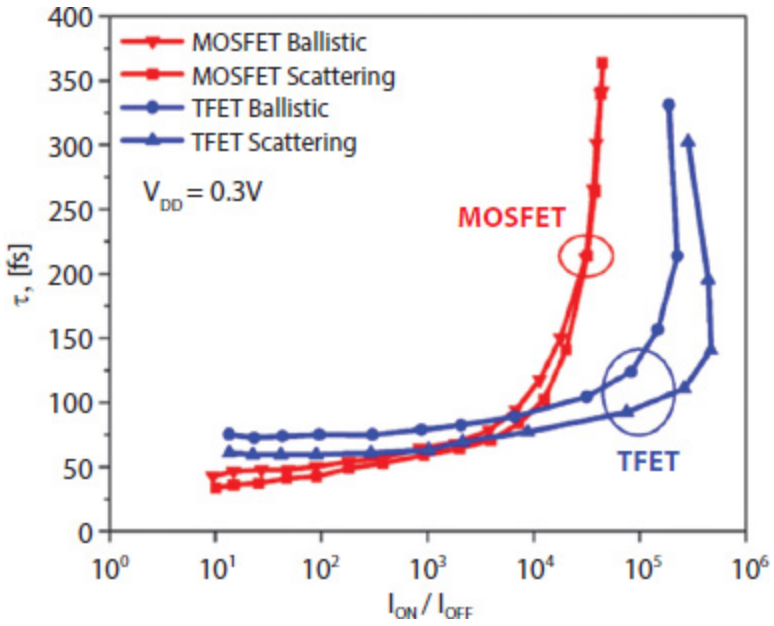

Figure 2.11 Comparison of intrinsic delay with I_{ON}/I_{OFF}.

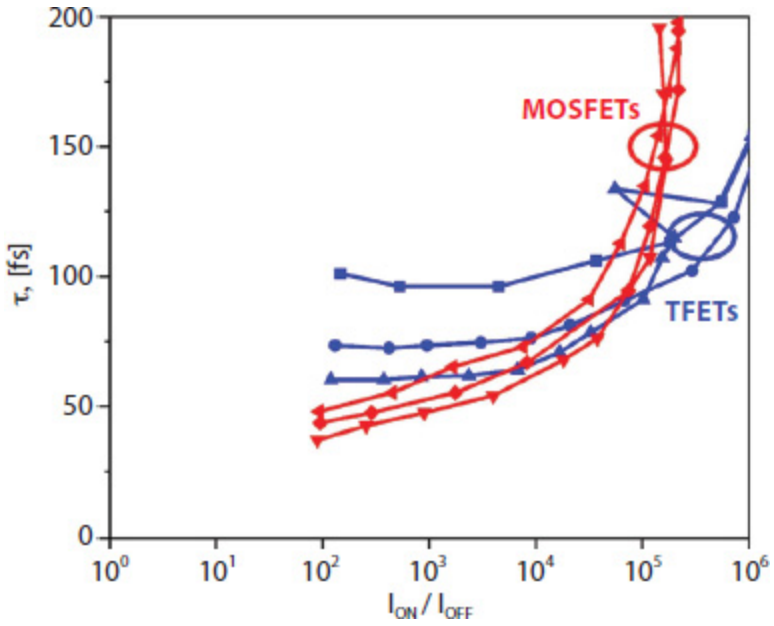

Figure 2.12 Device performance under dissipative transport in bandgap-dependent internal device delay.

Concerning narrow bandgap materials, ambipolar leakage is dramatically increasing for both TFETs and MOSFETs. The practical device-biasing range (V_{DD}) for materials with smaller bandgaps may be constrained if methods to reduce I_{OFF} are not discovered. The use of lightly doped drain extensions and heterojunction tool designs with a small bandgap cloth only

at the supply tunnelling area and a wider bandgap material in the channel and drain areas to reduce I_{OFF} are two examples of practical solutions in the case of TFET [17]. Due to these strategies, small bandgap materials will experience increased forward tunneling efficiency.

Each power delay product (PDP) has a minor effect on bandgap in the context of MOSFETs. MOSFET tool latency is somewhat decreased due to carriers' lower channel transit time [17, 18]. The lower effective mass and higher band speed of CNTs enables this to be supplied. We see a significant deterioration inside the framework of TFETs for large bandgap CNTs.

A decrease in tunnelling current, which negatively affects the switching velocity of such devices, is the leading cause of this. On the other hand, it could be connected to the lower injection charge for materials with large bandgaps at the tunneling junction. However, the bandgap dependence of PDP on TFETs is far less pronounced. More importantly, TFETs maintain their advantage in switching strength and, consequently, $P_{dynamic}$ even though fundamental disparities between MOSFETs and TFETs still exist in respect to PDP curves [18, 19].

2.11 MOSFET and TFET Scaling Behaviour

For the MOSFET and TFET, Figure 2.13 shows a curve of SS vs. temperature. The SS is decreased for each device to levels below 10mV/dec. Due to thermionic emission, a similar image implies the standard thermal line. At lower temperatures, the TFET and MOSFET will have a similar linear temperature dependency. A thermal injection is another possible component of TFET. Even though they significantly surpass the ideal circumstances, MOSFET SS ranges exhibit a linear trend [20]. In TFET, only below a temperature of 150K does the linear scaling of SS values occur. Since different types of devices have the same gate stack and channel material [22], interface state density (D_{it}) may affect them. As well as InGaSb/ InGaAs, tunnel junction may be the source of the TFET's higher SS for temperatures below 150K compared to the MOSFET. The SS for the TFET at room temperature may improve based on these results.

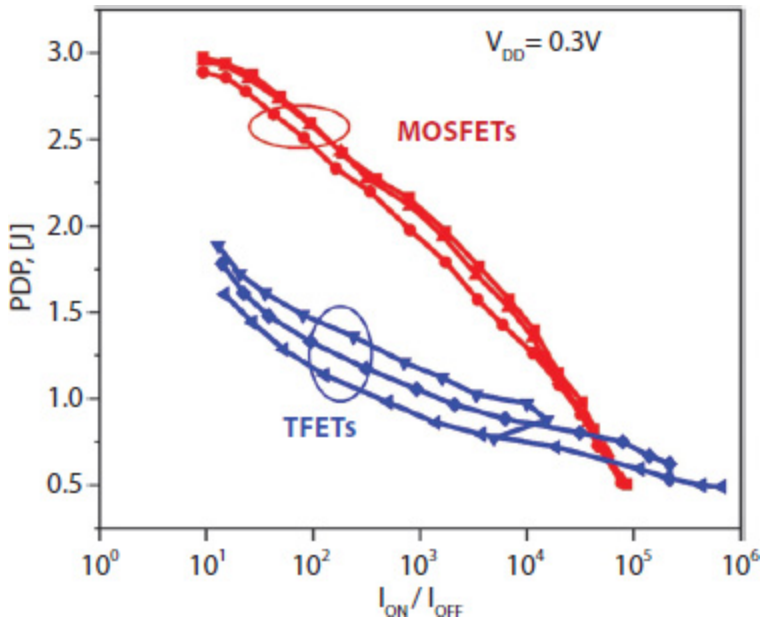

Figure 2.13 Device performance under dissipative transport is bandgap-dependent at PDP.

While MOSFETs have an immediate growing tendency in current times with smaller L_G, there is no apparent correlation for TFETs, as shown in Figure 2.14. The channel's conductance is often affected by the gate bias in TFETs, increasing BTBT with a decrease in tunnel barrier. The gate bias in a MOSFET frequently affects the tunnel junction's width [20, 21]. In a TFET, the tunneling resistance predominates the resistance between the supply and drain. Hence, it is not necessarily anticipated that the channel period would affect the I_D. The channel resistance's contribution to the total resistance could not be negligible over longer channel lengths, resulting in an L_G dependency for the I_D.

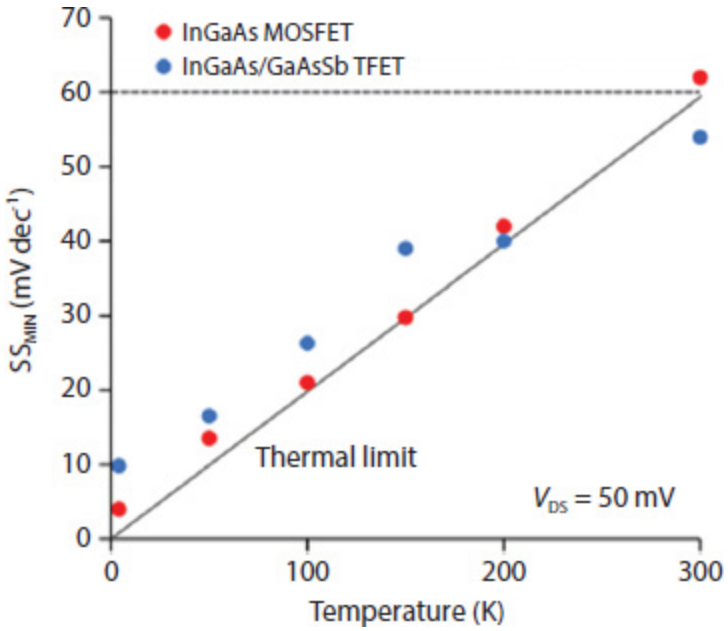

Figure 2.14 SS vs. temperature comparison of MOSFET and TFET.

2.12 Surface Potential of an N-TFET and N-MOSFET

As V_{DS} increases, the drain current of the MOSFET reaches its maximum value. This feature applies to the ON/OFF operation of the gadget. As the drain bias increases, the surrounding electric field is sufficient to reverse the bias of the J_{DC}. As a result of the channel's drain end being crushed, saturation occurs. The output characteristics of a TFET indicate that the drain current saturates as V_{DS} increases. Comparing a TFET and MOSFET with similar architecture reveals that the former has a larger drain voltage or point where the drain current is at its peak. Therefore, the o/p characteristics of a TFET saturate later than those of a standard transistor.

Surface potential is the potential difference between the Si and SiO2 interfaces in a device channel. It is expressed as a ratio to the zero-point Fermi level ($\Psi = 0$) at the source. Its lateral electric field at the drain channel junction (J_{DC}) of a TFET is lower than that of a MOSFET under identical biassing conditions (Figure 2.15). Both TFETs and MOSFETs have the same amount of charge in the channel when the gate is turned off [23]. For either type of device, the lateral electric field needed to pinch off

the channel at the J_{DC} is the same. Due to the increased V_{DS}, the linear portion of the o/p characteristics is lengthened. Because of this, a TFET's output characteristics reach saturation earlier than a MOSFET of the same structure (Figure 2.16).

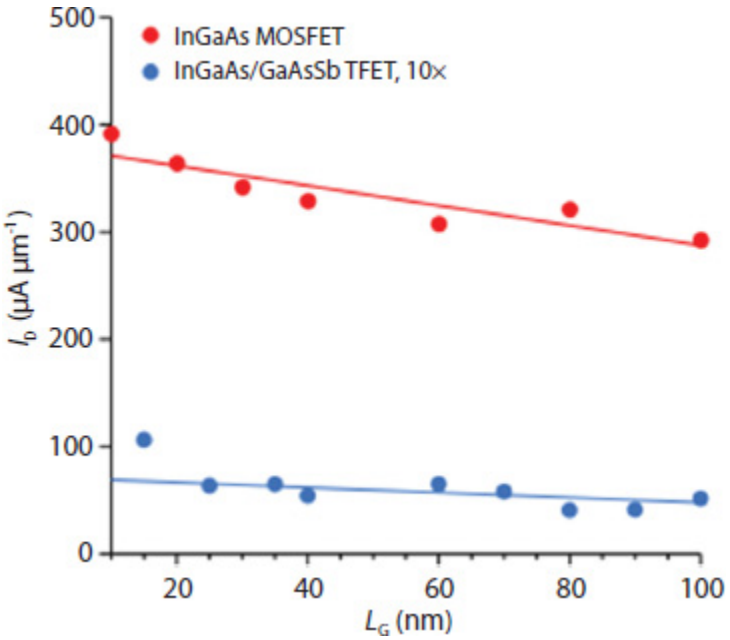

Figure 2.15 Drain current comparison.

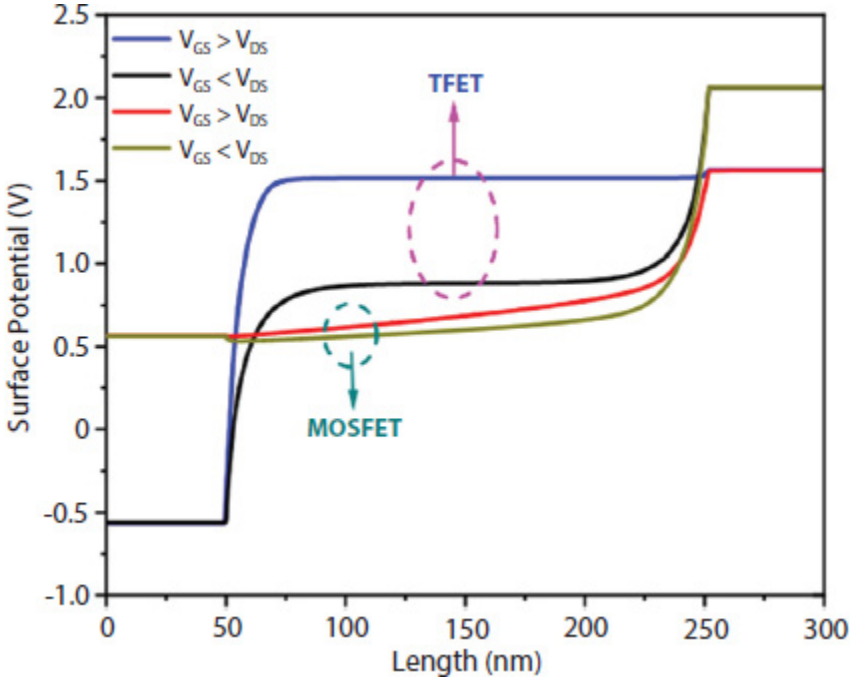

Figure 2.16 Surface potential of N-TFET and N-MOSFET.

2.13 Professional Advantages of TFET over MOSFET

- The TFET has a lower sub-threshold swing (SS) than the MOSFET at room temperature, which is 60 mV/dec or less.
- Unlike regular MOSFET, TFET only requires a small amount of power. As a result, they consume less energy and are suitable for ultra-low power applications.
- Eventually, III-V/Si heterojunction TFETs might be able to reach the level of steep slope switch.
- Conventional MOSFETs have a severe problem with power consumption as a result of scaling, but this is something that can be mitigated with TFETs.

2.14 Conclusion

The scaling rule was utilized to develop faster and more efficient MOSFETs. According to the scaling rule, the supply voltage for MOSFETs should go down as their numbers increase. However, subthreshold leakage has made this unlikely to occur. This has led to a lot of studies into steep subthreshold FETs. Tunneling FET is appealing for steep subthreshold FETs because of its simple structure and the drain voltage it can achieve. Thus, studying tunneling FETs, especially their on-state and subthreshold properties, is vital. Due to its foundational operating idea of BTBT, the TFET can attain a sub-60 mV/dec SS at room temperature. That's why it's a severe contender for fixing the power problems plaguing scaled MOSFET technology. The most challenging parts of TFET are getting the average SS down, the I_{ON} up, and the IOFF down. Group IV compounds, III-V materials, and 2D materials are all intriguing alternatives to silicon. When the materials are combined to produce a heterostructure, there are many possibilities for the device's fabrication. In addition to dopant pockets, optimizing the gate stack layout is another way to increase performance. By carefully deciding on the optimal material system, a well-designed device can improve the typical Si-TFET in output resistance, transconductance, ON current, and OFF current. Additionally, the sub-threshold swing (SS) is

lowered to a minimum at an average of 40mV/dec thanks to the TFET technology. System-on-Chip (SoC) applications are made possible and the performance of analog, digital, and RF components is improved. The gap between theoretical predictions and experimental findings suggests that there are still many problems to be fixed before the TFET can be used in low-power products.

References

1. J. Ajayan, D. Nirmal, Dheena Kurian, P. Mohankumar, L. Arivazhagan, A. S. Augustine Fletcher, T. D. Subash, and M. Saravanan**,** "Investigation of impact of gate underlap/overlap on the analog/RF performance of composite channel double gate MOSFETs" Journal of Vacuum Science & Technology, B vol.37, no.062201, 2019

2. M. Saravanan, Eswaran Parthasarathy, " A Review of III-V Tunnel Field Effect Transistors for Future Ultra Low Power Digital/Analog Applications" Microelectronics Journal, vol. 114 , no. 105102, 2021

3. Darshana V, Balamurugan N B and Arun Samuel T S, "An Analytical Modeling and Simulation of Surrounding Gate TFET with an Impact of Dual Material Gate and Stacked Oxide for Low Power Applications", Journal of Nano Research, vol. 57, no. 68, 2019

4. Ramkumar K and Ramakrishnan V N, " Performance Analysis of Germanium-Silicon Vertical Tunnel Field-Effect Transistors (Ge-Si-VTFETs) for Analog/ RF Applications", Silicon 1, 2022

5. Sathish kumar, M., Samuel, T. A., Ramkumar, K., Anand, I. V., & Rahi, S. B. "Performance evaluation of gate engineered InAs–Si heterojunction surrounding gate TFET" Superlattices and Microstructures, vol 162, no. 107099, 2022

6. Bhagwan Ram Raad, Dheeraj Sharma, Pravin Kondekar, Kaushal Nigam & Sagar Baronia "DC and analog/RF performance optimisation of source pocket dual work function TFET" International Journal of Electronics, Volume 104, no. 12, 2017

7. Saravanan M; Eswaran Parthasarathy, “Investigation of RF/Analog Performance of InAs/InGaAs Channel Based Nanowire TFETS” DOI: 10.1109/ICCISc52257.2021.9484973, 2021

8. Naima, G., Rahi, S. B., & Boussahla, G, “Impact of Dielectric Engineering on Analog/RF and Linearity Performance of Double Gate Tunnel FET”, International Journal of Nanoelectronics & Materials, vol,14, no.3, 2021.

9. Bhagwan, Dheeraj Sharma, Kaushal Nigam and Pravin Kondekar 2017 Group III–V ternary compound semiconductor materials for unipolar conduction in tunnel field-effect transistors Journal of Comp. Electronics vol.16, no. 24, 2017

10. C. K. Pandey, D. Dash & S. Chaudhury, “ Improvement in Analog/RF Performances of SOI TFET Using Dielectric Pocket” International Journal of Electronics, International Journal of Electronics, 2020, vol.107,11, pp 1844-1860

11. Saravanan M, Eswaran Parthasarathy, “Investigation of RF/Analog performance of Lg=16nm Planner In0.80Ga0.20As TFET” DOI: 10.1109/ ICECCT52121.2021.9616769, September 2021.

12. Pravin, Nirmal D, Prajoon P and Ajayan J, “ Implementation of nanoscale circuits using dual metal gate engineered nanowire MOSFET with high-k dielectrics for low power applications”, Phys. E Low-dimensional Syst. Nano. vol.83, no. 95, 2016

13. Mahdi Vadizade 2022 Digital Performance Assessment of the Dual-Material Gate GaAs/InAs/Ge Junctionless TFET IEEE Transactions on Electron Devices 68 1986

14. T.S. Arun Samuel and N.B. Balamurugan and S. Bhuvaneswari and D. Sharmila and K. Padmapriya , “Analytical modelling and simulation of single-gate SOI TFET for low-power applications” International Journal of Electronics, vol.106, 6, pp 779-788, 2014

15. Guenifi, N., Rahi, S. B., & Larbi, M, “Suppression of Ambipolar current and analysis of RF performance in double gate tunneling field

effect transistors for low-power application” Int J nanoparticles nanotech, vol.6, no. 33, 2020

16. S. O. Koswatta, M. S. Lundstrom, and D. E. Nikonov, “Band-to-band tunneling in a carbon nanotube metal–oxide–semiconductor field-effect transistor is dominated by phonon-assisted tunneling,” Nano Lett., vol. 7, no. 5, pp. 1160–1164, 2007.

17. A. Vassighi and M. Sachdev, “Thermal runaway in integrated circuits,” IEEE Trans. Device Mater. Rel., vol. 6, no. 2, pp. 300–305, 2006.

18. Ramkumar K, Ramakrishnan VN, “Investigation of Hetero Buried Oxide and Gate Dielectric PNPN Tunnel Field Effect Transistors” Silicon, vol.1, no.8, 2020

19. Ramkumar, K., Shailendra, S. R., & Ramakrishnan, V. N. “Performance Analysis of Carbon Nanotube and Graphene Tunnel Field-Effect Transistors. In Semiconductor Devices and Technologies for Future Ultra Low Power Electronics”, CRC Press, pp. 87-113, 2021

20. Anand, I. V., Samuel, T. S., Ramakrishnan, V. N., & Ram Kumar, K.,” Influence of trap carriers in SiO2/HfO2 stacked dielectric cylindrical gate tunnel FET”, Silicon, 1-12, 2021

21. Usha, C., Vimala, P., Ramkumar, K., & Ramakrishnan, V. N, “Electrostatic characteristics of a high-k stacked gate-all-around heterojunction tunnel field-effect transistor using the superposition principle” Journal of Computational Electronics, vol.1, no.10, 2022

22. M.Saravanan, Eswaran Parthasarathy, J.Ajayan, Nirmal, Chapter-5; “Impact of Semiconductor Materials and Architecture Design on TFET Device Performance”, Book: Emerging Low-power semiconductor devices: Applications for future technology nodes, CRC Press 2022.

23. Saravanan M, Eswaran Parthasarathy, Ramkumar K, “Performance Analysis of InAs-GaAs Gate-all-around Tunnel Field Effect Transistors (GAA-TFET) for Analog/ RF applications”, Journal of Physics: Conference Series, vol. 2335, no. 012043, 2022

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3
Operation Principle and Fabrication of TFET

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Abstract

Field-effect transistors, or FETs, are utilized in various electrical applications. Nanoelectronic circuits based on FETs, on either hand, are inefficient in terms of energy consumption since switching applications requires a high supply voltage. We have briefly reviewed the effect of TFETs against conventional MOSFETs from several viewpoints in this study. The supply voltage of conventional FETs, constrained by the subthreshold swing restriction of 60 mV/decade, can be reduced using tunnel FETs, a novel FET (SS) form. TFETs' capacity to achieve an inverted sub-threshold swing (SS) less than that of traditional MOSFETs' 60 mV/decade thermal limit (at 300 K) is their most noticeable characteristic. Despite conventional thermal injection, a TFET uses quantum mechanically based band-toband tunneling to transport charge carriers in device channels. Comparing thin semiconducting sheets or nanowires (TFETs) to complementary metal-oxide-semiconductor (CMOS) transistors, the power consumption of TFETs can be lowered by a factor of 100. As a result, combining TFETs and CMOS techniques to develop low-power integrated circuits could be advantageous. The newest TFET devices with multiple semiconducting channels and geometries are extensively investigated in this review, followed by a brief discussion of the persistent challenges in developing high-performance devices. Finally, career prospects for device design and TFET efficiency are addressed.

***Keywords*:** TFET, subthreshold swing, band-to-band tunneling (BTBT)

3.1 Introduction

The most common device structure in contemporary integrated circuits (ICs), including microprocessors and semiconductor memory devices, is the metal-oxide-semiconductor (MOS) system. Modern digital circuits almost exclusively use n-channel MOS field-effect transistors (MOSFETs) and complementary MOSFETs for massive-scale integration (MSI) and ultra-large-scale integration (ULSI) [1, 2].

Practical components that heavily rely on the MOS structure include charge-coupled devices (CCDs), insulated-gate field-effect transistors (IGFETs), and MOS field-effect transistors (MOSFETs) [3]. Si-SiO_2 technology is used to manufacture the bulk of MOSFETs and CCDs that are sold commercially. In ULSI circuits, MOSFETs are easily scaled-down and utilize very little power [4].

The physical and electrical characteristics of semiconductor surfaces and numerous IC applications have extensively employed the MOS structure. Since a MOSFET's dependability and stability are directly tied to the circumstances of the semiconductor surface, understanding the physical and electrical features of a semiconductor surface is essential for improving the performance of MOS devices [5].

The invention of the vacuum tube in the early twentieth century brought a new era to the electronics industry [6]. Solid-state switches were created shortly after to deal with the issues of vacuum tubes. Since then, efforts have been undertaken to reduce production costs while scaling transistor geometry and increasing package density. This geometric and architectural scaling enhanced chip operating frequencies, while reducing the chip cost per transistor [7–10]. The static power density in a device that is off is greater than the active power density, according to strict dimension scaling (device in ON state). MOSFETs have undergone numerous developments during the 1990s to enhance performance while eliminating scaling-related negative effects. Geometry scaling was once responsible for sub-threshold degradation, however, this is no longer the case [8, 11]. The power supply voltage should be reduced as the power density of MOSFETs is diminished [12]. To maintain the device's power performance and quick speed, the power supply and threshold voltage must be downsized in proportion to the channel length [13]. One of the most challenging technological issues is reducing subthreshold swing (SS), which is required to keep a high ON-state current while allowing for tolerable OFF-state leakage [14]. On the other hand, lowering the threshold voltage increases the OFF current (I_{OFF}), increasing the device's static power dissipation to an unacceptable level. As a result, the fundamental minimum SS of 60 mV/ dec limits the threshold voltage scaling of MOSFET devices [8, 15].

One form of developing technology is the tunneling field-effect transistor (TFET) [16]. A MOSFET is typically utilized in low-energy electronic devices. Although it has a different key switching mechanism, the tunneling field-effect transistor's structure is identical to that of a MOSFET; TFETs switch by changing quantum tunneling across a barrier as opposed to normal MOSFETs, which do so by modulating thermionic emission over a barrier [17]. The TFET's fundamental structure is a gated PIN diode and gate-controlled band-to-band tunneling governs how it functions. It is superior to MOSFETs in several ways, including being better suited for low power applications due to reduced outflow current, enhanced resilience to short channel effects, increased operating speed due to tunneling, and a noticeably lower threshold voltage and lower on/off current ratio. In light of this, TFET can be considered a competent substitute for MOSFET in applications requiring high speed and low power [18].

The overdrive voltage cannot be decreased by lowering the threshold voltage proportionally to the supply voltage, as depicted in Figure 3.1. When the supply voltage is scaled too high, the device has less driving current, which slows it down.

Over the last decade, the most significant drawback for the electronics industry and transistor scaling has been power consumption [19].

As a result, the nanoscalability of MOSFET threshold voltage has two critical repercussions:

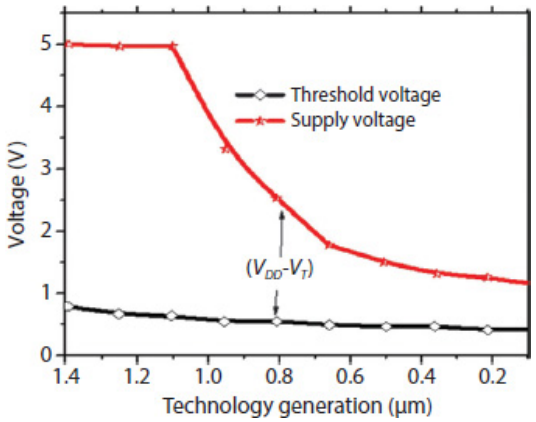

Figure 3.1 Trends in supply voltage scaling and threshold voltage based on international semiconductor technology roadmap [8].

Table 3.1 Supply voltage scaling trend at various technology nodes [8].

Node (nm)	500.00	350.00	250.00	180.00	130.00	90.00	65.00	45.00	20.00
V_{DD} (V)	5.00	3.30	2.50	1.80	1.30	1.20	1.1	1.00	0.6

I. The reduction in overdrive voltage reduced supply voltage scaling, as indicated in Table 3.1.

II. By scaling the transistor size without increasing the supply voltage, the electric field inside the channel grows, which causes an increase in the leakage current.

3.2 Planar MOSFET's Limitations

Device geometry scaling improves performance while reducing device size and power consumption [19]. To preserve device dependability and electrostatic integrity, transistors are scaled in terms of channel length, source/ drain junction depth, channel width, gate oxide thickness, channel doping concentration, transistor pitch, connection, and power supply [20].

3.2.1 Effects of Short Channels

The "Short Channel Effect" (SCE), which decreases gate control and has undesirable effects, is brought on by the source's close proximity to the channel [21]. One of these effects is drain-induced barrier lowering (DIBL), which happens when the drain bias controls the drain current [22]. Weak gate electrostatics, a rise in OFF-state current, and a decrease in ON current are some of the features of short channel effects [22]. Planar MOSFETs display a poor subthreshold swing (>80mv/dec) and a much higher OFF current (>100nA/m) when the gate length is scaled below 30nm, despite significant technological obstacles [23]. Thus, scaling of planar bulk MOSFETs is getting more and more challenging.

The "Short Channel Effect" (SCE), which results in less gate control and unwanted outcomes is brought on by the close proximity of the source and the channel. Drain-induced barrier lowering, one of these situations when the drain bias influences the drain current, is known as DIBL [24]. Weak gate electrostatics, a rise in OFF-state current, and a decrease in ON current are further impacts of tiny channels. Despite severe technical challenges, planar MOSFETs exhibit a poor subthreshold swing (>80mv/dec) and a significantly higher OFF current (>100nA/m) when the

gate length is scaled below 30nm. Planar bulk MOSFET scaling is thus made more difficult. At room temperature, the SS of MOSFETs cannot be lowered to 60 mV/dec even in the ideal case of unlimited gate capacitance [25]. Impact-ionization MOS devices, nanoelectromechanical FETs, suspended gate MOSFETs, and tunneling FETs (TFETs) can all achieve a sub-60 mV/ dec SS [26–29].

Tunnel field-effect transistors (tunnel FETs), as opposed to metal oxide semiconductor field-effect transistors (MOSFETs), turn on and off via electron tunneling [25]. In contrast to the MOSFET, which employs thermal carrier injection, the TFET uses band-to-band tunneling as its source carrier injection method [30]. The TFET can achieve sub-60 mV/ dec SS because it uses a different source carrier injection strategy than the MOSFET does [15, 31, 32].

3.3 Demand for Low Power Operation

Modern business operations and consumer needs for data acquisition, processing, and entertainment drive the growing industrial demand for creating, acquiring, storing, processing, and transmitting information. The issue started with the introduction of the electronic calculator, personal computer, and microprocessor-driven games. The increased need for computing, combined with growing demand, has resulted in integrated circuits that are faster, smaller, more dependable, and less powerful. The technology accompanying these advancements can be incorporated into the combatant's electronic systems to improve functionality and reduce battery consumption. The industry has embarked on a long-term strategy to mitigate electronic devices' size and operating voltages while increasing device and circuit integration. We are studying the National Technology Roadmap systems for Semiconductors (NTRS) in technological advancement. Integrated circuits (ICs) further lowered power usage by allowing multiple devices to be packed on a single chip, eliminating the interconnection constraint and minimizing power consumption [33]. An invented complementary metal-oxide-semiconductor (CMOS) integrated circuit was the crucial low-power CMOS device used as a building block in most Ics for significantly lower Ics power consumption [34]. Future life quality depends on the perspective improvements of information technology. In the field of sensing technology, highly desirable products like house monitoring (air pollution, humidity, fire, temperature, human health, security), traffic monitoring (car speed, traffic jams, accidents), agricultural monitoring (air pollution, temperature, humidity, wind, lightning, rain, storms), space monitoring (stars, sun, meteorites, moon, other astronomical phenomena), security monitoring, and so on have been created by many companies.

Three primary applications that drive the demand for low-power FET electronic devices are:

i. Portable electrical goods, including wristwatches, cardiac pacemakers, personal digital assistants, hearing aids, pocket calculators, etc.

ii. Improved performance by increasing the package density of components in integrated circuits while countering power consumption restrictions

iii. Power preservation in desktop computers with a modest life cycle cost-to-performance ratio, which necessitates low power for cheaper power supply and cooling expenses (34); low utilization of power results in lower chip temperatures, higher stability, and less expensive plastic packages [35].

The power consumption of dynamic random access memory (DRAM) circuits can be significantly lower. Power dissipation challenges in electronic systems are treated at many levels. Out of the different hierarchies in electronic systems, only device issues relating to low-power electronics are discussed, like circuits, materials, devices, and procedures.

To know low-power electronics, one must first understand the components of integrated circuits or semiconductor devices. The MOS-field-effect transistor (MOSFET), which is used in low-power circuits, is the cornerstone of CMOS [5]. N-type and P-type transistors are used in silicon CMOS technology [36]. The predominant semiconductor technology currently utilized in memory, microprocessors, and application-specific integrated circuits is CMOS technology [37, 38]. This allows a reduction in the voltage supply without sacrificing performance by increasing the turn-on steepness, which means lowering the average SS below the SSmin. Steep-slope switches are expected to enable successful power scaling. Different device topologies, such as tunnel FETs (TFETs), are being researched due to the limitations of MOSFETs.

3.4 TFET: Operation Principle of TFET

Maintaining Moore's Law over the next decade will necessitate continued scaling of transistor physical dimensions, performance enhancement, and aggressive power reduction [39]. Scaling channel lengths beyond 10nm has become exceedingly challenging as Moore's law approaches its limits because direct tunneling between the source and drain lowers gate control and switching capacity and increases power dissipation [40]. Luckily, new device topologies like TFETs and the use of new materials with peculiar properties have expanded the range of possible circuit designs [41]. For nanoelectronic circuits, power consumption is a significant issue. As a result, lowering V_{DD} is required to reduce power consumption [42, 43]. However, a considerable reduction in V_{DD} has a substantial impact on MOSFET performance [44]. The speed at which the transistor switches from being off to being on as a function of gate voltage is the problem [45]. At room temperature, the thermionic effect in subthreshold MOSFETs requires a minimum of 60 mV to increase the current by order of magnitude [29].

Due to its excellent electrical properties, such as its low subthreshold swing (less than 60 mV/dec) and high ON/OFF current ratio with low OFF leakage current in complementary metal-oxide-semiconductor (CMOS) technology, the tunneling field-effect transistor has drawn a lot of attention from researchers [32, 46]. Due to their low OFF leakage current, tunnel FETs are ideal for low-power, very large-scale integration (VLSI) applications [46]. Since they can produce a subthreshold swing of less than 60 mV/decade, tunnel field-effect transistors (TFETs) are one of the next-generation options to compete with CMOS transistors at low voltage operation [40].

The MOS device known as the tunnel field-effect transistor (TFET) uses band tunneling between transistors (BTBT) [45]. The SS of the TFET operates extraordinarily efficiently at very low voltage thanks to the device's fundamental conduction mechanism, function at sub-60-mv/dec [18, 47].

In contrast to a MOSFET where free carriers from the source cross the source-channel barrier on the application of drain voltage, free carriers in a TFET are created due to band-to-band tunneling across the source-channel junction and are then swept towards the drain due to the applied drain electric field [48]. A TFET's operation is dependent on quantum mechanical processes, therefore, naturally, modeling for a TFET differs from modeling for a MOSFET [1, 49]. Non-equilibrium Green Function (NEGF) modeling provides the foundation for most atomistic modeling of TFETs.

Quantum effects are markedly more pronounced because atomistic modeling is far more trustworthy and accurate, especially at small device dimensions [48].

The tunnel field-effect transistor (TFET) uses MOS technology known as band tunneling between transistors (BTBT) [45]. The SS of the TFET may operate with exceptional efficiency at very low voltage thanks to the device's basic conduction mechanism, a sub-60-mv/dec operation [18, 47]. This device is a potential low-power substitute since its basic switching process varies from a metal-oxide-semiconductor field-effect transistor (MOSFET) [42]. TFETs switch using quantum tunneling over a barrier, as opposed to conventional MOSFETs, which switch through thermionic emission over a barrier [50].

The MOSFET drain current subthreshold swing is capped at around 60 mV/decade of current because TFETs are unaffected by the thermal Maxwell-Boltzmann carriers at ordinary temperatures [44]. TFETs are more resistant to short-channel problems than conventional nanoscale MOSFETs because the tunneling mechanism keeps the channel current on the source site [39, 42]. Therefore, gate-controlled pin topologies with carriers tunneling through rather than flowing over the barrier are used in the most promising TFETs.

While TFETs switch by modifying quantum tunneling over a barrier, conventional MOSFETs switch by modifying thermionic emission across a barrier. An n-type TFET's intrinsic area is activated by applying gate bias, which causes electron accumulation [50]. Band-to-band tunneling (BTBT) occurs when the intrinsic region's conduction band and the P region's valence band collide at a substantial gate bias [51]. Current can flow through the device because electrons from the p-type region's valence band tunnel into the intrinsic region's conduction band. When the gate bias drops, bands stray from alignment and block current flow [16, 52].

Tunnel field-effect transistors (TFETs), which are lauded as potential alternatives for energy-efficient transistors, frequently employ band-toband tunneling (BTBT) [44]. The central injection uses band-to-band tunneling (BTBT) as an alternative to MOSFETs that thermally inject charge carriers over a potential barrier [53]. The transition of charge carriers occurs between energy bands. However, due to switching applications requiring a high supply voltage, nanoelectronic circuits based on FETs are inefficient in terms of energy use [31]. The subthreshold swing (SS) (TFETs) constraint of 60 mV/decade limits the supply voltage in conventional FETs; tunnel FETs are a novel type of FET developed to get around this restriction [51].

Quantum tunneling between the source and channel generates a current. Current transport events in the tunnel FET type of field-effect device are brought on by quantum tunneling between the source and channel [24]. Figure 3.2a depicts the TFET's operation. The sources, drain, and gate terminal voltages are denoted by V_S, V_D, and V_G, respectively. To understand how TFET functions are made more accessible by the band-diagram, we have provided illustrations in Figures 3.2b and c. Figure 3.2c shows the location of the energy bands at thermal equilibrium and when the drain-to-source voltage is reverse-biased (V_{DS}). When the gate experiences a constant positive drain-to-source voltage ($V_G = 0$), the component behaves as a reverse-biased p-i-n diode. BTBT and thermionic emission are both strongly impeded by design under this bias, as seen in Figure 3.2. This barrier allows a minute amount of off-state current to pass through the device, simulating reverse saturation on a p-i-n diode.

When a positive V_G is used, the electron concentration causes the bands in the channel area to bend downward [26]. When the conduction band of the channel area is narrower than the valence band of the source region, BTBT occurs at the p+ channel junction.

As seen in Figure 3.2c, electrons can also tunnel from the valence band of the p+-doped zone to the conduction band of the region with electron accumulation. This illustration also demonstrates how using V_G causes the formation of a potent electric field and a narrow tunneling zone at the p+-intrinsic junction.

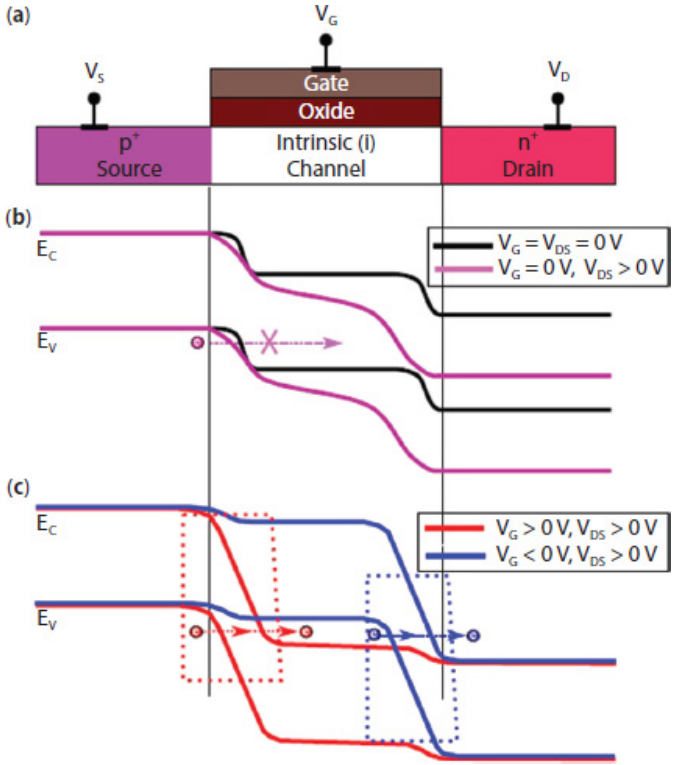

Figure 3.2 TFET operation: The internal structure of the transistor, band alignment under reverse V_{DS}, and thermal equilibrium of the transistor are all thoroughly explained in a. In b and c, the band alignment for positive and negative V_G is also covered. The dotted patches indicate the tunneling zone in the diagram [53].

Only in the tunneling window, which is an area where complete energy levels compete with empty energy states of equal energy, does tunneling take place [30, 32]. As V_G grows, a significantly accumulated electron channel, like those in MOSFETs, “pins” the channel potential to the drain potential [51]. As V_G approaches the drain potential, the band bending in the channel area does not dramatically alter. As a result, the tunneling current reaches saturation and essentially stabilizes. Only within the tunneling window, where total energy levels compete with empty energy states of equal energy, does tunneling take place [30, 32]. When V_G increases, a MOSFET or other strongly accumulated electron channel will “pin” the channel potential to the drain potential [51]. As V_G approaches the drain potential, the band bending in the channel area does not dramatically alter. Slight variations and tunneling current saturation occur as a result.

The channel develops holes and the bands in the channel region considerably arc when the V_{GS} is negative. Electrons can tunnel from the valence band of the channel region to the conduction band of the n+-doped region thanks to the intrinsic-n+ junction’s strong electric field and constrictive tunneling zone. As stray electrons from the valence band of the p+-doped area fill the channel openings, a current flows from the p+-doped site to the n+-doped region.

Due to the high concentration of holes in the channel, the bands in the channel area become pinned to the source potential when the V_G magnitude reduces adversely. When V_G reaches the source potential, the channel area moves to a higher saturation, but the tunneling current does not change significantly.

A schematic illustration of (a) MOSFET and (b) TFET devices is shown in Figure 3.3), which depicts a cross-sectional view of a MOSFET and a TFET. The source area, which controls carrier injection from source to channel, is the sole part of the design that differs. A TFET is a gated P-i-N diode that operates as a tunneling diode while ON and as a reverse bias diode when OFF. High I_{ON}/I_{OFF} is made possible by the asymmetry of the structure and the tunneling of carriers, but this also prevents source-drain exchange which is beneficial for MOSFETs.

Figure 3.4 contrasts the operating variations between MOSFET and Tunnel FET. TFET injects carriers from source to channel, as opposed to MOSFET which injects carriers thermionically through the barrier because of gate field-induced band-to-band tunneling (BTBT). Because carrier tunneling is impossible, a shallow leakage current is maintained and the valence band of the source and the conduction band of the channel are not in alignment. The gate field lowers the conduction band of the channel area to align it with the valance band of the source region in the ON state. By reducing the tunneling barrier's breadth and height, this alignment enables carrier injection and tunneling from the source region to the channel region. When the bands coincide, TFET devices can function well below sub-thermionic thresholds and provide a quick turn-on with sub-threshold swing values below 60 mV/dec. When a minority carrier is injected, the TFET's substantially more significant barrier for minority carriers lowers leakage current in the OFF state [54]. The majority of the leakage current that does occur in TFET devices is regulated by SRH recombination and trap-aided tunneling (TAT), even though it is much smaller than leakage in MOSFET devices with shorter channel lengths [54].

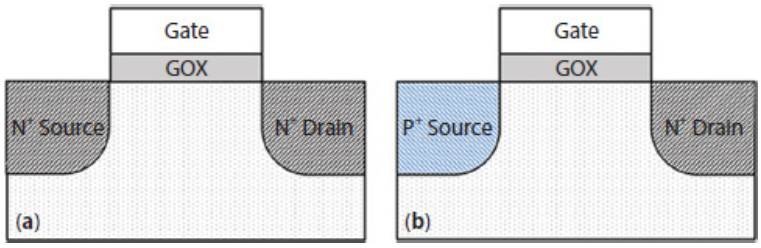

Figure 3.3 Schematic illustration of (a) MOSFET and (b) TFET devices.

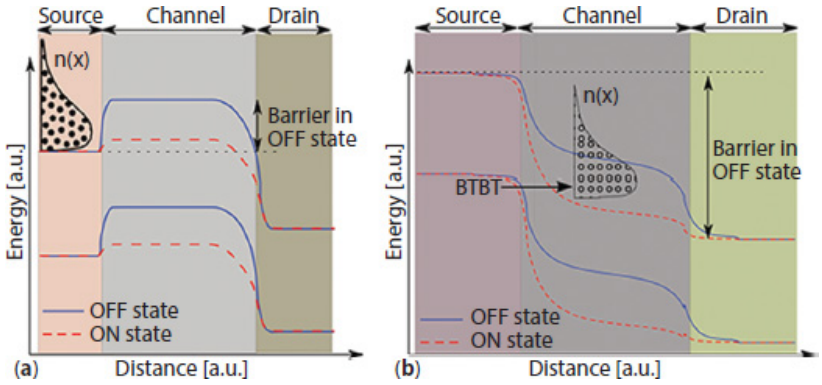

Figure 3.4 Energy band diagrams of (a) MOSFET and (b) TFET in the ON and OFF states, which highlight the significant distinction between band-to-band tunneling and thermionic injection [54].

The conventional/gated P-i-N TFET layouts can reduce leakage, allow voltage scaling, and compensate for short channel effects, however, they have a low ON current. Recently, this device has frequently been referred to as a point TFET, as shown in Figure 3.5a.

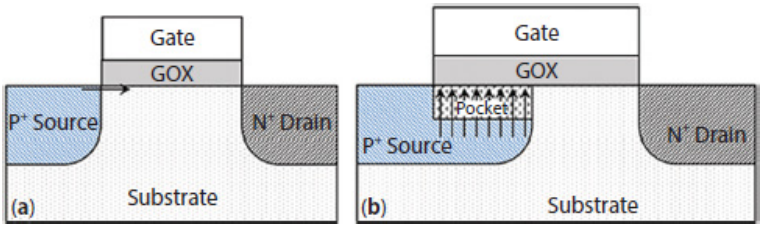

Figure 3.5 Structural and functional distinctions between (a) line TFET and (b) pocket layer TFET.

The ON current of a TFET is negatively correlated with its cross-section and a likelihood of tunneling (TBTBT) [48, 54]. The expression for the tunneling probability produced by WKB, using a triangular barrier to approximate the tunnel barrier, is as follows:

$$T_{BTBT} = exp\left(\frac{-4\lambda\sqrt{2m^{*}E_g^3}}{3q\hbar\left(E_g+\Delta\Phi\right)}\right) \approx exp\left(\frac{-4\sqrt{2m^{*}E_g^3}}{3q\hbar F}\right) \quad (3.1)$$

where λ is the screening tunneling length, which is dependent on the particular device form and identifies the location of the transition zone at the source-channel interface. A common technique for reducing SRH leakage is to use low bandgap material only at the tunnel junction. m* stands for effective tunneling mass, Eg for material bandgap, and F for the electric field. The device's remaining components are constructed from materials that have a relatively wider bandgap. A heterojunction TFET, excluding the tunneling junction, is another name for it (low bandgap source area for N-type devices and common bandgap channel region for P-type devices).

The cross-sectional tunnel area and tunneling course are represented by the arrows and their densities [54].

The performance of the line TFET is highly impacted by source engineering and pocket layer design. The bandgaps, doping of the source and pocket layers, and the thickness of the pocket region serve as design requirements [55]. It could be said that pocket engineering uses more control to create devices for various applications. A line TFET architecture's compatibility with CMOS and ease of integration using CMOS unit production stages should be noted [54].

3.5 TFET: Recent Design Issues in TFET

3.5.1 TFET: Subthreshold Swing Perspective

Tunnel field-effect transistors (TFETs) perform better than complementary metal-oxide semiconductors (CMOS) in applications needing low supply voltage [41]. However, the subthreshold swing is essential when modeling the weak inversion area, particularly for high-gain analog applications, imaging circuits, and low-voltage applications [32, 41]. Band-toband tunnel FETs are a viable alternative for next-generation low-power digital applications because they feature a smaller subthreshold swing and lower OFF-current than traditional metal-oxide-semiconductor field-effect transistors. Because they can produce subthreshold swing (SS) below

60 (MOSFETs), band-to-band tunnel FETs are being investigated as a competitive substitute for traditional metal-oxide-semiconductor field-effect transistors (MOSFETs) [15]. The lower SS of TFETs leads to a substantially larger on-current at a lower supply voltage, less leakage, and enhanced low-voltage performance because thermionic emission is not utilized in this device [47, 56].

One of the so-called steep-slope devices being investigated for use in extremely low-power electronic applications is the tunnel field-effect transistor (TFET) [49]. The ability of the TFET to support an inverted sub-threshold slope, S, below the threshold limit of 60 mV/dec for conventional FETs is a critical characteristic necessary for low-power switching [32, 57].

One of the most critical performance criteria for the device is sub-threshold swing (SS), which is defined as [15, 25, 58]:

$$SS = \left(\frac{d\,logI_{ds}}{d(\Delta E / g)} \right)^{-1} = \frac{SS_T SS_{FD}}{SS_T + SS_{FD}} \tag{3.2}$$

where $SS_T = \left(\frac{d\,log(T(\Delta F))}{d(\Delta E / g)} \right)^{-1} = \frac{2\sqrt{2}\,ln(10)\hbar}{-q\pi\sqrt{m_T E_g \frac{dW_T}{d\Delta E}}}, SS_{FD} = \left(\frac{d\,log(F_{Integral})}{d(\Delta E / g)} \right)^{-1}$ *and* $\vec{F}$ is the electric field at the junction [15], modeled as $\vec{F} = E_g/W_T$, the reduced planks constant is $\hbar$, minimum tunnel width is W_T, and allowable tunnel window transportation energy is ΔE.

It has a minimum value, as indicated in Equation 3.2.

$$SS_{min} = \frac{k_\beta T}{e} ln(10) = 60mV / dec \tag{3.3}$$

Here, T is the temperature at 300 K, K_β is the Boltzmann constant, and e is the absolute value of the electron charge.

The subthreshold swing of the TFET device is restricted to 48 mV/ dec, which is less than that of a MOSFET device, as shown in Figure 3.6, for various oxide thicknesses of MOSFET and TFET. In this graph, the DIBL rises along the length of the channel while the subthreshold swing falls.

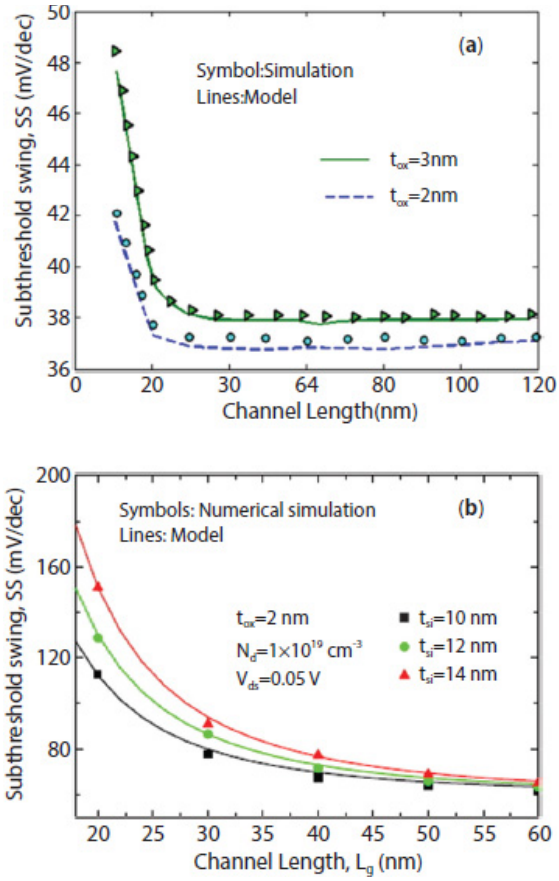

Figure 3.6 SS versus channel length comparison for various oxide thicknesses in a) GAA heterojunction tunnel field-effect transistors [41] and b) short channel JL-DG_MOSFET [58].

3.5.2 TFET: Power Consumption Perspective

One fascinating steep subthreshold slope technology being researched to reach beyond the power density and energy efficiency restrictions of CMOS technology is the tunnel transistor [56, 59]. Low voltage functioning at a reasonable speed is made possible by a high subthreshold slope (SS), which results in power and energy savings [60]. They are therefore being investigated to find solutions to CMOS's power density and energy efficiency issues because of its minimal subthreshold slope of 60 mV/decade. Tunnel-FET technology has recently been a contender to bypass supply voltage scaling restrictions in ultra-low power applications [47]. Our review shows numerous studies have compared TFET transistors to CMOS transistors in logic applications. As demonstrated, speed improvement with TFET-based synthetic circuits at ultra-low voltages comes at the cost of increased power consumption. TFET-based MSP processors used 34.8 percent less power than FinFET-based MSP processors at supply voltages as low as 200 mV [47].

Table 3.2 displays the noise margin as a percentage of supply voltage for several TFET and FinFET-based logic gates operating at 200, 300, and 400 mV. Because of the asymmetry of this device, changing the supply voltage affects the noise margin of TFET-based cells, as opposed to FinFET-based equivalents, which maintain their robustness better when the supply voltage is changed.

3.6 TFET: Modeling and Application

3.6.1 TFET: Modeling

To model the TFET, the device's surface potential must be solved first. As a result, let's start by looking at the simulation findings for the TFET's surface potential and an analogous MOSFET's surface potential. Calculations must be made to determine the surface potential and constant potential values at the source-channel junction.

To reproduce the surface potential, let's write the two-dimensional Poisson equation in the TFET channels [48]:

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2}=\frac{qN_A}{\varepsilon_{Si}} \tag{3.4}$$

Table 3.2 Displays the noise margin for FinField effect transistors and tunnel field-effect transistor-based INV, NOR_2, NOR_3, $NAND_2$, and $NAND_3$ gates at 200, 300, and 400 mV, normalized to 50% of the supply voltage [47].

V_{DD}(mV)	FinFET					TFET				
	INV	**NOR_2**	**NOR_3**	**$NAND_2$**	**$NAND_3$**	**INV**	**NOR_2**	**NOR_3**	**$NAND_2$**	**$NAND_3$**
0.2	70.80%	69.20%	67.70%	72.30%	72.50%	66.00%	65.00%	65.00%	68.00%	69.00%
0.3	77.60%	77.60%	77.50%	80.50%	80.90%	74.00%	75.50%	75.00%	77.40%	78.10%
0.4	81.20%	81.20%	81.20%	84.50%	84.50%	67.00%	62.30%	60.00%	65.40%	66.70%

where N_A denotes the doping concentration of the TFET channel. It is crucial to solve this equation to model a TFET. Numerous mathematical techniques, presumptions, simplifications, and approximations are used to compute the two-dimensional (2D) Poisson equation.

For example, since the 2D Poisson equation is solved using the parabolic approximation, Equation 3.4 can be considerably approximated by a parabolic function [48].

At y=0:

$$\frac{\partial^2\psi(x,y)}{\partial x^2}-\frac{C_{OX}}{t_{si}\varepsilon_{Si}}\psi_S(x)=\frac{qN_A}{\varepsilon_{Si}}-\frac{C_{OX}}{t_{si}\varepsilon_{Si}}\psi_S(x) \tag{3.5}$$

The homogeneous part of Equation 3.4 is

$$\frac{\partial^2\psi(x,y)}{\partial x^2}-\frac{C_{OX}}{t_{si}\varepsilon_{Si}}\psi_S(x)=0 \tag{3.6}$$

Equation 3.5 has a general solution form, shown below:

$$\psi_S(x)=C\exp\left(\frac{X}{L_d}\right)+D\exp\left(\frac{-X}{L_d}\right) \tag{3.7}$$

where L_d is the characteristic length given by:

$$L_d = \sqrt{t_{Si}\varepsilon_{Si} / C_{OX}} = \sqrt{t_{Si}t_{OX}\varepsilon_{Si} / C_{OX}} \tag{3.8}$$

Another solution to Equation 3.4 is

$$\psi_S(x) = \psi_G - \frac{qN_A L^2{}_d}{\varepsilon_{Si}} \tag{3.9}$$

Therefore, the final solution of Equation 3.4 using the particular and homogenous solution is given by:

$$\psi_S(x) = C\ exp\left(\frac{X}{L_d}\right) + D\ exp\left(\frac{-X}{L_d}\right) + \psi_G - \frac{qN_A L^2{}_d}{\varepsilon_{Si}} \tag{3.10}$$

The general form solution for a TFET's surface potential is given by Equation 3.9. Thought the surface potential of a TFET's available form is given by Equation 3.9, but our work is far from done. There are two unknown coefficients in Equation 3.9: C and D. These coefficients will be solved using the x-direction boundary conditions.

3.6.2 TFET: Application

TFETs', or Tunnel FETs', fabrication processes are similar to MOSFETs' because they have similar applications, such as a digital switch [61]. The applications of TFETs, also known as tunnel FETS, and MOSFETs, such as a digital switch, are comparable [49]. Low-off currents make them ideal for low-power applications that operate at moderate frequencies and low-standby-power logic. Low-power SRAM and ultra-low-power customized analog ICs (integrated circuits) with increased temperature resistance are two other applications for tunnel FETS [62]. TFETs operate on a very distinct set of principles from MOSFETs [57]. While the conduction process in Tunnel FETs is connected to Zener tunneling, the flow of current in MOSFETs will be caused by diffusion phenomena [57]. Research on TFET, a collection of devices with an intermediate frequency steep slope, is being done for extremely low-power applications [49]. Low standby industrial metering, telemetry, asset and vehicle monitoring, wireless security systems, and other applications are suited for them due to their low currents [57]. The TFET is a member of the so-called steep slope device family which is now being investigated for use in ultra-low-power electronic applications [41]. For instance, numerous memory devices can be created by fusing TFET with MOSFET and PCM. The p-i-n structure of the TFET is advantageous for applications in memory areas, which lessens the importance of the TFET's low I_{DS} [57].

3.7 TFET: Fabrication Perspective

A technique for creating a tunneling field-effect transistor (TFET) device is disclosed in yet another embodiment. A gate structure with a gate and a gate dielectric is formed on a substrate made of a first substrate material as part of the process. Near the gate structure, the first kind of drain zone and an intermediate source region are generated. The source region is positioned beneath the gate dielectric so that at least a piece of it overlaps the gate dielectric. The process involves selecting and almost eliminating the intermediate source region, creating a cavity below the gate dielectric positioned between the substrate and the gate dielectric and exposing some substrates. On the exposed portion of the substrate, a first source region is created and a second

source region is formed above it. The second source region is different from the first source region and at least a portion of both the first and second source regions is located inside the cavity.

The fabrication processes of TFET are illustrated in Figure 3.7. The source area of a semiconductor device used to fabricate a TFET device has at least a portion of it located below a gate dielectric. According to one design, the TFET has a silicon substrate with an N- drain area and a P+ source region, where the N- drain region is silicon and the P+ source region is silicon germanium (SiGe). At least a portion of the source area is positioned below the gate dielectric and it consists of a first region of a first type (P+SiGe) and a second region of a second type (undoped SiGe). This design narrows the tunneling barrier and boosts the drive current (I_D).

The device is shown after (a) STI on SOI substrates is used to define the active area; (b) Si is etched back, followed by the growth of a p+ SiGe source and an i-Si pocket; (c) gate stack deposition and etching; and (d) source protection using silicon nitride is applied, the drain window is opened, and the source material is etched back [63].

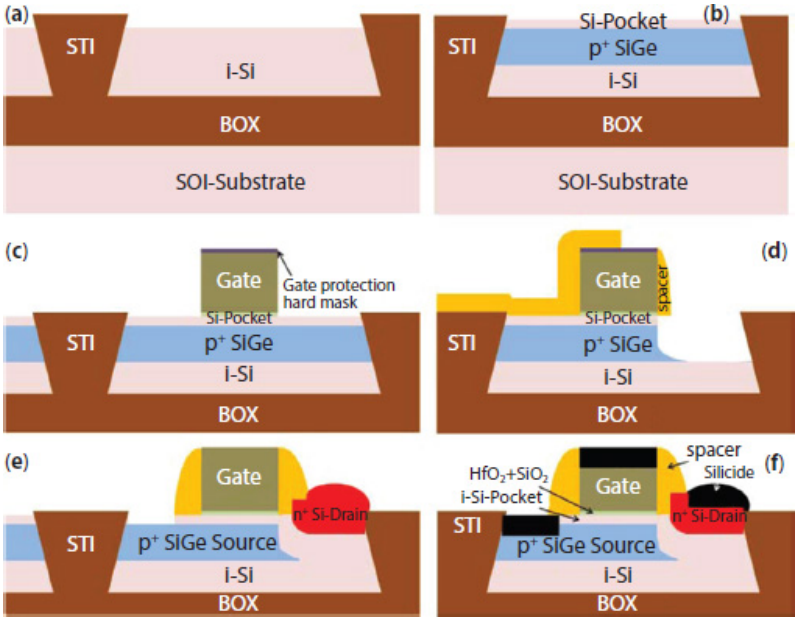

Figure 3.7 Fabrication steps for TFET.

3.8 TFET: Applications and Future of Low-Power Electronics

Emphasis is placed on the effects of several critical TFET characteristics, including unidirectional conduction, delayed saturation, and higher Miller capacitance, as well as the functioning and resilience of logic and SRAM circuits [64]. Memory device applications are one of the TFET's unique electrical characteristics [57]. Another illustration uses TFET as the access transistor for phase change memory cells [57]. It is shown that TFET logic circuits and structural improvements in device design make it easier to construct small circuits and increase their performance.

3.9 Expected Challenges in Replacing MOSFET with TFET

The preliminary step in developing a biosensor is ultra-small scale device fabrication in recent technology. Nowadays, fabricating mass production, highly sensitive, real-time measurement

capability, label-free electrical sensors, and cost-effective, scalable biosensors with low power-driven TFETs is a perfect candidate for various medical and basic scientific research projects [65]. However, using current large-scale fabrication technologies, individual nanostructures cannot be consistently placed on a substrate [39]. As a result, Bandgap engineering, on-state performance enhancement, and current production procedures, which are highly vulnerable to processing conditions and probabilistic nanostructure positioning, produce nano-TFET devices with significant unpredictability and device-to-device inconsistency. Some of the essential encounters faced in the development of TFETs are that the current properties are asymmetric and potentially uncontrolled, making circuit design problematic [66]. The imbalanced and unregulated current of the TFET affects the transmission gate and circuits using a transmission gate structure, such as the SRAM bitcell [41, 43]. The tunnel field-effect transistor (TFET) has a steep-slope potential and benefits from functioning at low supply voltage, making it a potential future transistor [40]. Research has been done on the forward p-i-n current of the TFET because it substantially impacts circuit performance [39, 41]. The density-of-states (DOS) expanding past the bandgap (bandtail) as a result of excessive doping density is another non-ideality concern [49]. The non-homogeneous distribution of dopant atoms causes this phenomenon, which results in differing local potentials than a homogeneous distribution [66].

The forward p-i-n current significantly increases static power consumption and decreases the hold static noise margin (HSNM). The layout density, source/drain asymmetry, requirement for high-quality materials, and need for oxides with minimal body dimensions of the TFET are all obstacles to commercialization. Furthermore, compared to the MOSFET, the TFET has higher trap-induced deterioration [43]. High-quality materials and oxides are necessary to counteract the effects of trap-assisted tunneling, as are minimal body dimensions. Furthermore, the layout density and circuit reliability problems are worsened by the source/drain asymmetry of TFETs [42]. Continued studies will concentrate on finding solutions to these problems so that TFETs can offer longer battery life while sacrificing some chip space, which is crucial for highly parallelizable products.

3.10 Conclusion

This study examined TFET and conventional MOSFET-based circuits in subthreshold swing and energy consumption for ultra-low-voltage operation. As a result, it may be possible to circumvent the challenges associated with estimating precisely how much TFET energy is saved when V_{DD} is reduced compared to CMOS technology. Since power and delay (frequency) are the two most important design factors, these designs are provided. On TFET performance and benefits, the impacts of switching activity, logic depth, and minimum supply voltage have also been discussed. According to this study, TFETs are the best steep-slope switch replacement. It may function at low supply voltages of less than 0.5 V, resulting in significant reductions in power dissipation. Their low-off currents are appropriate for applications needing external power logic, low standby power, and running at moderate rates. Two other potential TFETs include ultra-low-power specialized analog integrated circuits and lowpower SRAM with improved temperature stability. The subthreshold slope for both traditional MOSFETs and TFETs is highlighted in this review and it is clear that the TFET subthreshold slope is less than 60 mv/decade. As a result, tunnel FETs are appropriate for low-power applications. Four characteristics of TFET’s in-circuit issues include the layout’s essential active area qualities, low on-current, delayed output saturation, and unmanageable forward p-i-n current of the gate.

Several issues must be resolved to achieve fantastic performance (high I_{ON}) without lowering I_{OFF} and an S of less than 60 mV per decade with more than four decades of drain current. As a result, the technological boosters currently in use or being developed must be blended additively.

Finally, we proposed using TFETs as inexpensive, disposable, and portable chips because of their low power requirements and lowered subthreshold slope of less than 60 mv/decade. Under low supply voltage conditions, tunnel field-effect transistors (TFETs) outperform equivalent metal oxide semiconductor transistors, making them a suitable replacement for MOSFETs.

References

1. Park KY, Kim MS, Choi SY. Fabrication and characteristics of MOSFET protein chip for detection of ribosomal protein. Biosens Bioelectron. 2015;20(10 SPEC. ISS.):2111–5.

2. Georgiev VP, Dochioiu AI, Lema FA, Berada S, Mirza MM, Paul DJ, *et al.* Variability study of high current junctionless silicon nanowire transistors. In: 2017 IEEE 12th Nanotechnology Materials and Devices Conference, NMDC 2017. 2018. p. 87–8.

3. Lin R, Lu Q, Ranade P, King T, Hu C. An Adjustable Work Function Technology Using Mo Gate for CMOS Devices. IEEE ELECTRON DEVICE Lett [Internet]. 2002;23(1):49–51. Available from: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=1004233

4. Li SS. Semiconductor physical electronics. Second Edi. United States of America.: Springer Science+Business Media, LLC; 2006. 708 p.

5. Saha P, Banerjee P, Dash DK, Sarkar SK. Impact of trapped interface charges on short channel characteristics of WFE high-K SOI MOSFET. Proc 3rd Int Conf 2019 Devices Integr Circuit, DevIC 2019. 2019;118–23.

6. Gautam R, Saxena M, Member S, In A, Mosfet GAA. Numerical Model of Gate-All-Around MOSFET With Vacuum Gate Dielectric for Biomolecule Detection. IEEE ELECTRON DEVICE Lett VOL 33, NO 12, DECEMBER 2012. 2012;33(12):1756–8.

7. Adnan MMR, Hafiz MS Bin, Tasneem N, Khosru QDM. Quantum ballistic transport in ultra-small silicon channel cylindrical gate-all-around junctionless nanowire transistor using NEGF formalism. 2016 IEEE Int Conf Electron Devices Solid-State Circuits, EDSSC 2016. 2016;62–5.

8. Dubey PK. Tunnel FET : Devices and Circuits [Internet]. Nanoelectronics. Elsevier Inc.; 2019. 1-26 p. Available from: http://dx.doi.org/10.1016/B978-0-12-813353-8.00002-6

9. MOSFET Scaling Crisis and the Evolution of Nanoelectronic.

10. Jacobson ZA. Band-to-Band Tunneling Transistors: Scalability and Circuit Performance. Vol. 53, Journal of Chemical Information and Modeling. University of California, Berkeley; 2012.

11. Dhiman G. Investigation of Junction - less Double Gate MOSFET With High - k Gate - oxide and Metal Gate Layers. Int J Innov Res Sci Eng Technol. 2019;8(6S3):289–92.

12. Gupta N, Chaujar R. Impact of Device Parameter Variation on RF Performance of Gate Electrode Workfunction Engineered (GEWE) - Silicon Nanowire (SiNW) MOSFET. 2015; (June).

13. Kumar S, Paliwal KK, Mahajan S. EFFECT OF REDUCTION IN GATE OXIDE 100NM MOSFET. Int J Latest Res Sci Technol. 2018;7(1):5–8.

14. Wang X, Shahidi G, Oldiges P, Khare M. Device scaling of high performance MOSFET with metal gate high-K at 32nm technology node and beyond. Int Conf Simul Semicond Process Devices, SISPAD. 2008;309–12.

15. Cao W, Sarkar D, Khatami Y, Kang J, Banerjee K. Subthreshold-swing physics of tunnel field-effect transistors. AIP Adv [Internet]. 2014;4(6). Available from: http://dx.doi.org/10.1063/1.4881979

16. Ajay, Gupta M, Narang R, Saxena M. Analysis of GaSb-InAs Gate all around (GAA) p-i-n tunnel FET (TFET) for application as a bio-sensor. 2016 IEEE Int Nanoelectron Conf. 2016; (June 2013):1–2.

17. Chandan BV, Nigam K, Sharma D, Pandey S. Impact of interface trap charges on dopingless tunnel FET for enhancement of linearity characteristics. Appl Phys A Mater Sci Process [Internet]. 2018;124(7):1–6. Available from: http://dx.doi.org/10.1007/s00339-018-1923-8

18. Toh EH, Wang GH, Samudra G, Yeo YC. Device physics and design of double-gate tunneling field-effect transistor by silicon film thickness optimization. Appl Phys Lett. 2007;90(26).

19. Transistor MF, Taur Y. ULSI Scaling Toward 10nm Gate-lengths: Challenges and Opportunities. 2019;

20. Siddik AB, Hossain NMM, Quader S, Chowdhury MIB. Silicon on metal technology merged with cylindrical gate all around FET for enhanced performance. 3rd Int Conf Electr Inf Commun Technol EICT 2017. 2018;2018–Janua(December):1–4.

21. Rony MW, Bhowmik P, Myler HR, Mondol P. Short channel effects suppression in a dual-gate gate-all-around Si nanowire junctionless nMOSFET. Proc 9th Int Conf Electr Comput Eng ICECE 2016. 2017;538–41.

22. Getnet Yirak M, Chaujar R. TCAD Analysis and Modelling of Gate-Stack Gate All around Junctionless Silicon NWFET Based Bio-Sensor for Biomedical Application. In: Proceedings of 2nd International Conference on VLSI Device, Circuit and System, VLSI DCS 2020. 2020. p. 18–9.

23. Arora N. MOSFET MODELING FOR VLSI SIMULATION Theory and Practice [Internet]. World Scientific Publishing Co. Re. Ltd. 5 Toh Tuck Link, Singapore 596224 USA office: 27 Warren Street, Suite 401-402, Hackensack, NJ 07601 UK office: 57 Shelton Street, Covent Garden, London WC2H 9HE. 2007. Available from: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6634225

24. Naima G, Rahi SB. Design and Optimization of Heterostructure Double Gate Tunneling Field Effect Transistor for Ultra Low Power Circuit and System. Electr Electron Devices, Circuits, Mater. 2021;19–36.

25. Qiu Y, Member S, Wang R, Huang Q, Member S. A Comparative Study on the Impacts of Interface Traps on Tunneling FET and MOSFET. IEEE Trans Electron Devices. 2014;61(5):1284–91.

26. Jang JS, Choi WY. Ambipolarity factor of tunneling field-effect transistors (TFETs). J Semicond Technol Sci. 2011;11(4):272–7.

27. Li W, Liu H, Wang S, Chen S, Han T, Yang K. Design and investigation of dopingless dual-gate tunneling transistor based on line tunneling. AIP Adv [Internet]. 2019;9(4). Available from: http://dx.doi.org/10.1063/1.5087879

28. Teherani JT. Band-to-band Tunneling in Silicon Diodes and Tunnel Transistors. University of Texas at Austin; 2008.

29. Sarkar D, Banerjee K. Proposal for tunnel-field-effect-transistor as ultra-sensitive and label-free biosensors. Appl Phys Lett. 2012;100(14).

30. Lin J, Antoniadis DA, Del Alamo JA. Off-state leakage induced by band-toband tunneling and floating-body bipolar effect in InGaAs quantum-well MOSFETs. IEEE Electron Device Lett. 2014;35(12):1203–5.

31. Choi WY, Park B, Lee JD. Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec. 2007;(September).

32. Singh A, Chaudhary S, Sharma SM, Sarkar CK. Improved Drive Capability of Silicon Nano Tube Tunnel FET Using Halo Implantation. Silicon. 2020;12(11):2555–61.

33. Omura Y, Mallik A, Matsuo N. MOS Devices for Low-Voltage and Low-Energy Applications. MOS Devices for Low-Voltage and Low-Energy Applications. South Tower, Singapore: WILEY; 2016. 1-465 p.

34. Technologies E, Committee DS, Power E, Soldier D, Isbn C, Pdf T, *et al.* Low Power Electronics and Design. In: Energy-Efficient Technologies for the Dismounted Soldier. 1997.

35. Gopalakrishnan K, Woo R, Jungemann C, Griffin PB, Plummer JD. Impact ionization MOS (I-MOS) - Part II : Experimental results. IEEE Trans Electron Devices. 2005;52(1):77–84.

36. Lu N, Gao A, Dai P, Mao H, Zuo X, Fan C, *et al.* Ultrasensitive Detection of Dual Cancer Biomarkers with Integrated CMOS-Compatible Nanowire Arrays. Anal Chem. 2015;87(22):11203–8.

37. Rony MW, Mondol P, Myler HR. Sensitivity of a 10nm dual-gate GAA Si nanowire nMOSFET to process variation. 19th Int Conf Comput Inf Technol ICCIT 2016. 2017;557–62.

38. Veera Boopathy E, Raghul G, Karthick K. Low power and high performance MOSFET. In: 2015 International Conference on VLSI Systems, Architecture, Technology and Applications, VLSI-SATA 2015. 2015.

39. Pandey R, Mookerjea S, Datta S. Opportunities and Challenges of Tunnel FETs. IEEE Trans Circuits Syst I Regul Pap. 2016;63(12):2128–38.

40. Chen K, Zhang Q, Li Y, Zhao J, Chen M. FreePDK15TFET : An Open-source Process Design Kit for 15nm CMOS and TFET devices.

41. Lin Z, Chen P, Ye L, Yan X, Dong L, Zhang S, *et al.* Challenges and Solutions of the TFET Circuit Design. IEEE Trans Circuits Syst I Regul Pap. 2020;67(12):4918–31.

42. Kumar MJ, Janardhanan S. Doping-less tunnel field effect transistor: Design and investigation. IEEE Trans Electron Devices. 2013;60(10):3285–90.

43. Avci UE, Morris DH, Young IA. Tunnel field-effect transistors: Prospects and challenges. IEEE J Electron Devices Soc. 2015;3(3):88–95.

44. Peesa RB, Panda DK. Rapid Detection of Biomolecules in a Junction Less Tunnel Field-Effect Transistor (JL-TFET) Biosensor. Silicon. 2021;4–10.

45. MOSFET short channel effects [Internet]. OnMyPhD. 2017. p. 1–5. Available from: http://www.onmyphd.com/?p=mosfet.short.channel.effects

46. Usha C, Vimala P, Samuel TSA, Pandian MK. A novel 2-D analytical model for the electrical characteristics of a gate-all-around heterojunction tunnel field-effect transistor, including depletion regions. J Comput Electron [Internet]. 2020;19(3):1144–53. Available from: https://doi.org/10.1007/s10825-020-01503-8

47. Rendón M, Cao C, Landázuri K, Garzón E, Prócel LM, Taco R. Performance Benchmarking of TFET and FinFET Digital Circuits from a Synthesis-Based Perspective. Electron. 2022;11(4):1–12.

48. Mamidala JK, Vishnoi R, Pandey P. Tunnel Field-effect Transistors (TFET): Modelling and Simulation. Tunnel Field-effect Transistors (TFET): Modelling and Simulation. 2016. 1-195 p.

49. Avci UE, Morris DH, Young IA. Tunnel field-effect transistors: Prospects and challenges. IEEE J Electron Devices Soc. 2015;3(3):88–95.

50. Kumar N, Raman A. Performance Assessment of the Charge-Plasma-Based Cylindrical GAA Vertical Nanowire TFET with Impact of Interface Trap Charges. IEEE Trans Electron Devices. 2019;66(10):4453–60.

51. Nazir G, Rehman A, Park SJ. Energy-Efficient Tunneling Field-Effect Transistors for Low-Power Device Applications: Challenges and Opportunities. ACS Appl Mater Interfaces. 2020;12(42):47127–63.

52. Ranjith R, Suja KJ, Komaragiri RS. An analytical model for a TFET with an n-doped channel operating in accumulation and inversion modes. J Comput Electron [Internet]. 2021;20(3):1125–36. Available from: https://doi.org/10.1007/s10825-021-01683-x

53. Verma M, Tirkey S, Yadav S, Sharma D, Yadav DS. Performance Assessment of A Novel Vertical Dielectrically Modulated TFET-Based Biosensor. IEEE Trans Electron Devices [Internet]. 2017;1–8. Available from: https://sci-hub.tw/https://doi.org/10.1109/TED.2017.2732820

54. Fet FT. Fin-Enabled-Area-Scaled Tunnel FET. 2015;62(10):3184–91.

55. Raad BR, Tirkey S, Sharma D, Kondekar P. A New Design Approach of Dopingless Tunnel FET for Enhancement of Device Characteristics. IEEE Trans Electron Devices. 2017;64(4):1830–6.

56. Avci UE, Rios R, Kuhn KJ, Young IA. Comparison of power and performance for the TFET and MOSFET and considerations for P-TFET. Proc IEEE Conf Nanotechnol. 2011;869–72.

57. Zang SG, Liu XY, Lin X, Liu L, Liu W, Zhang DW, *et al.* Applications of tunneling FET in memory devices. ICSICT-2010 - 2010 10th IEEE Int Conf Solid-State Integr Circuit Technol Proc. 2010;1238–40.

58. Jiang C, Liang R, Wang J, Xu J. A two-dimensional analytical model for short channel junctionless double-gate MOSFETs. AIP Adv. 2015;5(5).

59. Núñez J, Avedillo MJ. Comparison of TFETs and CMOS Using Optimal Design Points for Power-Speed Tradeoffs. IEEE Trans Nanotechnol. 2017;16(1):83–9.

60. Rewari S, Haldar S, Nath V, Deswal SS, Gupta RS. Numerical modeling of Subthreshold region of junctionless double surrounding gate MOSFET (JLDSG). Superlattices Microstruct [Internet]. 2016;90:8–19. Available from: http://dx.doi.org/10.1016/j.spmi.2015.11.026

61. Ghosh S, Chattopadhyay A, Tewari S. Optimization of Hetero-Gate-Dielectric Tunnel FET for Label-Free Detection and Identification of Biomolecules. IEEE Trans Electron Devices. 2019;67(5):1–8.

62. Biswal SM, Swain SK, Sahoo JR, Swain AK, Routaray K, Nanda U, *et al.* A comparative study of junctionless triple-material cylindrical surrounding gate tunnel FET [Internet]. Vol. 521, Lecture Notes in Electrical Engineering. Springer Singapore; 2019. 793-801 p. Available from: http://dx.doi.org/10.1007/978-981-13-1906-8_80

63. Walke AM, Vandooren A, Rooyackers R, Leonelli D, Hikavyy A, Loo R, *et al.* Fabrication and Analysis of a Si/Si0.55Ge0.45 Heterojunction Line Tunnel FET. IEEE Trans Electron Devices [Internet]. 2014;61(3):707–15. Available from: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6727530

64. Fan M, Chen Y, Su P, Chuang C. Challenges and Designs of TFET for Digital Applications.

65. Zheng C, Huang L, Zhang H, Sun Z, Zhang Z, Zhang GJ. Fabrication of Ultrasensitive Field-Effect Transistor DNA Biosensors by a Directional Transfer Technique Based on CVD-Grown Graphene. ACS Appl Mater Interfaces. 2015;7(31):16953–9.

66. Lenka TR. Micro and Nanoelectronics Devices, Circuits and Systems. 2021.

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4
Mathematical Modeling of TFET and Its Future Applications: Ultra Low-Power SRAM Circuit and III-IV TFET

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Abstract

Just as the human body is a complex engineering marvel consisting of a large number of cells, an integrated circuit is made up of millions of transistors. Following Moore's Law, dimensions of MOSFETs have been scaled down continuously to pack more transistors on a silicon wafer. Further scaling of MOSFETs poses a threat to the power limitations of electronic devices. The most promising alternative to MOSFETs is Tunnel Field Effect Transistors (TFET) because they can achieve a sub-threshold swing below 60mV/decade. This is due to the different current conducting mechanisms, namely tunneling in TFETs and thermionic injection in MOSFETs. In this chapter, we introduce the device architecture of TFETs that have been widely explored by various researchers.

The chapter continues with suitable modeling approaches developed to explore TFETs. These models give an insight into the device physics and justifies the competitive edge of TFETs over MOSFETs. The modeling approaches discussed are atomistic and analytical modeling. Further, we discuss the parabolic approximation of surface potential in TFETs and compare them with simulation results obtained by device simulation of TFETs using the TCAD tool Silvaco ATLAS. Finally, the applications of TFETs and the road ahead will be discussed.

Keywords**:** Low power consumption, low power operation, tunnel FET (TFET), modeling, device analysis, transistor analysis

4.1 Introduction

With the development of portable electronic devices (laptops, smart phones, the Apple watch and Galaxy watch, etc.), the demand for lowpower electronic devices has steadily increased. According to this demand, various research has been conducted among electrical engineers, material engineers, and electrical engineers. From the transistor level (low level), various device structures have been proposed including a cylindrical structure (GAA MOSFET), fin-shaped structure (FinFET), and double gate (DG) structure. However, structural development has clear limitations in that the structure of the channel is hard to freely change due to fabrication issues. Therefore, lots of research has been done to overcome these limitations.

Fortunately, researchers discovered a remarkable phenomenon that can significantly lower power consumption without changing the structure of the transistor. When the source and drain of the transistor have different dopant types (p^+ or n^+), the amount of current in the transistor is determined by a different principle. Specifically, when the source and drain of the transistor possess different dopant types, the electron in the channel moves via the band-to-band tunneling (BTBT) principle instead. Because of this BTBT, the transistor could achieve significant low on-current and off-current which enables low power operation. The proposed structure with different dopant types in the source and drain is called ‘Tunnel FET (TFET)’.

To analyze the performance and power consumption of TFET, various research has been broadly done through simulation and fabrication technologies. Simulation-based modeling approaches have a distinguished advantage in that they can perform in-depth analysis on TFET. From modeling approaches, researchers can analyze which physical mechanism determines the performance and power consumption of TFET. In this chapter, we are going to broadly analyze the various modeling approaches developed so far.

4.2 Modeling Approaches

The approach considered for modeling TFET is fundamentally different from that of MOSFETs as it is dependent on band-to-band tunneling of free carriers. Before understanding device-level modeling for TFET, it is reasonable to learn about the differences between MOSFET and TFET. Conduction in MOSFETs is due to thermionic emission and in TFETs is due to band-to-band tunneling. The sub-threshold swing is restricted to 60mV/decade in MOSFETs, but it is observed that TFETs have lower value. Generally, two approaches are considered for modeling: Atomistic Modeling and Analytical Modeling.

4.2.1 Atomistic Modeling

Atomistic modeling is based on a Non-Equilibrium Green function involving the extraction of energy bands using the Density Functional Theory. The Ballistic Transport model collaborates with the band structure to self-consistently solve the waveforms and allowable energy states [1].

Advantages of this modeling approach are that it is highly accurate and works for sub-nano-meter technology. But it involves a long duration of intensive computational calculations and the execution of it may take highly efficient processors. The mode space approach potentially reduces cost, as it is intensely difficult to obtain atomistic full-band models. As transistor dimensions are diminished to a few nanometers, quantum mechanical effects and details of atoms play a critical role in determining device physics. In open systems, the quantum process is determined by two methods, namely the Non-Equilibrium Green's function (NEGF) or Quantum Transmitting Boundary Method (QTBM)[2].

4.2.2 Analytical Modeling

Analytical modeling makes use of fundamental device physics and approximation to find a good final result for the device. The advantage of using an analytical approach is the requirement of less intensive computation without compromising on the accuracy of the results [3].

The approach followed for analytical modeling of TFET is shown in Figure 4.1.

The first step is to define and design the structure of TFET. TFETs are broadly classified as Planar TFET and non-planar/three dimensional TFET. Planar TFETs are single gate, double gate, double material gate, P-N-P-N, N-P-N-P, Hetero-junction, and Ferro-Electric TFET.

Non-planar TFETs are Gate All Around (GAA) TFET, Tri-gate/Fin-FET, CNT TFET, and Graphene TFET.

The second step is to represent the surface potential injunction between the source and channel. Poisson's equation (two dimension) is specified by:

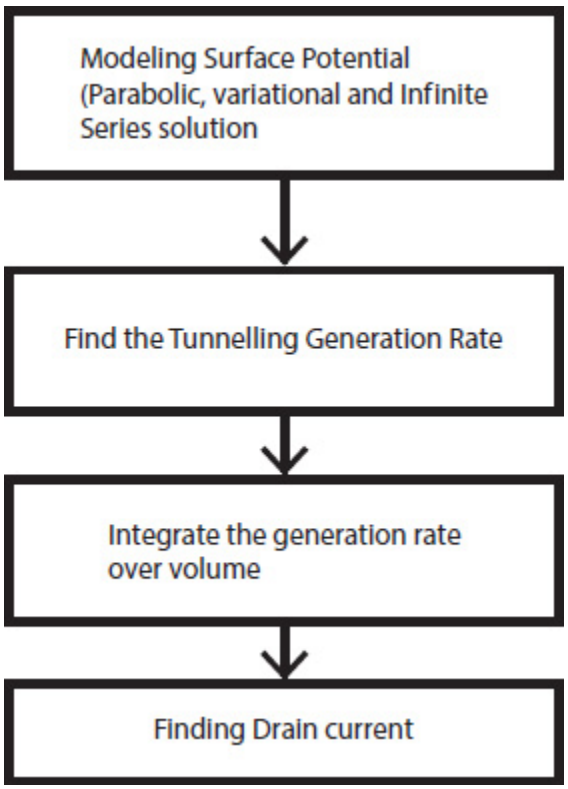
Modeling Surface Potential (Parabolic, variational and Infinite Series solution
Find the Tunnelling Generation Rate
Integrate the generation rate over volume
Finding Drain current

Figure 4.1 Procedure to find drain current using analytical modeling.

$$\frac{\partial^2 \Psi(x,y)}{\partial x^2} + \frac{\partial^2 \Psi(x,y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{Si}} \tag{4.1}$$

where N_A is the body doping of TFET. Since it is a second-order differential equation, it cannot be integrated directly.

Three methods or approximations are used, namely parabolic approximation, a variational approach, and an infinite series solution [3]. Pseudo-2D method is another name for parabolic approximation and it is

the most preferred modeling method followed where the Poisson equation discussed earlier is converted into a second-order one-dimensional linear differential equation [4].

4.3 Structure

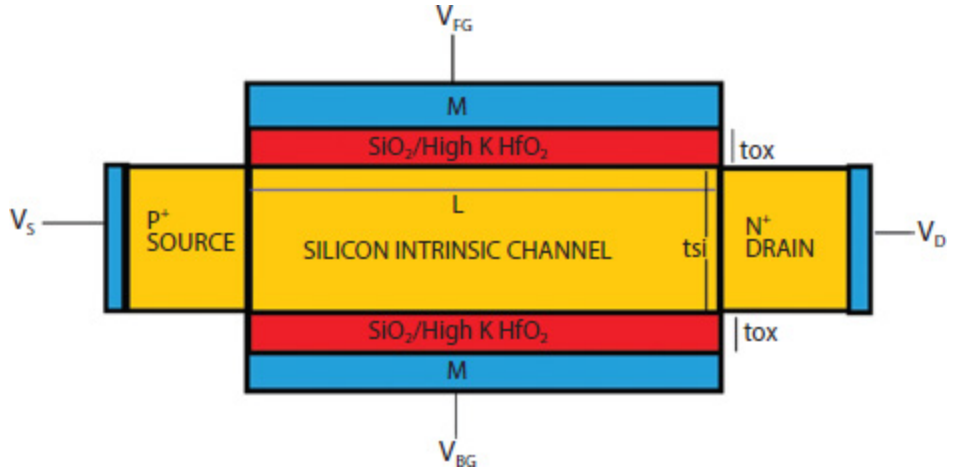

Figure 4.2 2D device structure of silicon dual gate silicon tunnel field.

4.3.1 Effect Transistor

Figure 4.2 illustrates the two-dimensional device structure of Dual Gate TFET. Dual gate offers better controllability of the channel and silicon is doped with p-type material to form a P+ source of 10nm, drain doped with n-type material that is also of 10nm. The intrinsic channel is of 20nm. The gate oxide thickness is of 1nm and the metal is considered for the gate electrode. The above device structure is simulated in the ATLAS Silvaco TCAD Simulator.

Potential distribution in Dual Gate TFET is depicted in the x and y direction in Figures 4.3 and 4.4, respectively. It can be observed in Figure 4.4 that surface potential is monotonous in nature and it is approximated as the below equation.

$$\Psi(x,y) = \Psi_s(x) + R_1(x)y + R_2(x)y^2_{\square} \tag{4.2}$$

The electric field at the body center is equal to zero and termed as the boundary condition. Also, the potential at the Silicon and di-electric

interface is equal to the surface potential and electric field displacement is continuous across the Silicon-dielectric interface.

The drain current obtained in DG Silicon TFET will be twice that of the single gate Silicon TFET. The drain characteristics are shown in Figure 4.5.

The second method used is the variational approach for modeling surface potential in TFET and the inversion characteristics effect is accounted for. Calculus is used and the 2D Poisson equation is converted into a Lagrangian function.

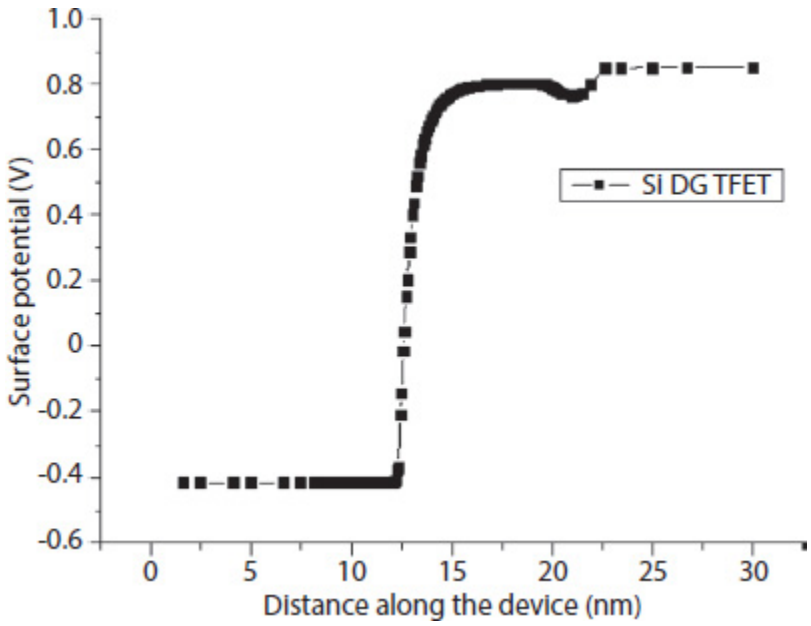

Figure 4.3 Distribution of surface potential along x-direction in silicon dual gate TFET.

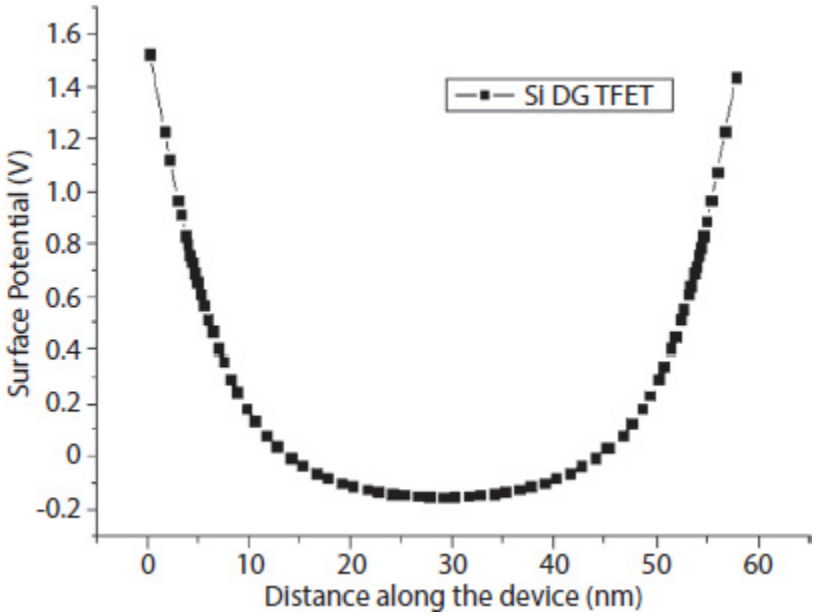

Figure 4.4 Distribution of surface potential along y-direction in silicon dual gate TFET.

The third method is used to realize surface potential using the separation of variables technique. This provides the infusion of infinite series solutions for potential. Even though it provides an accurate solution, it fails to give a closed-form solution for the surface potential.

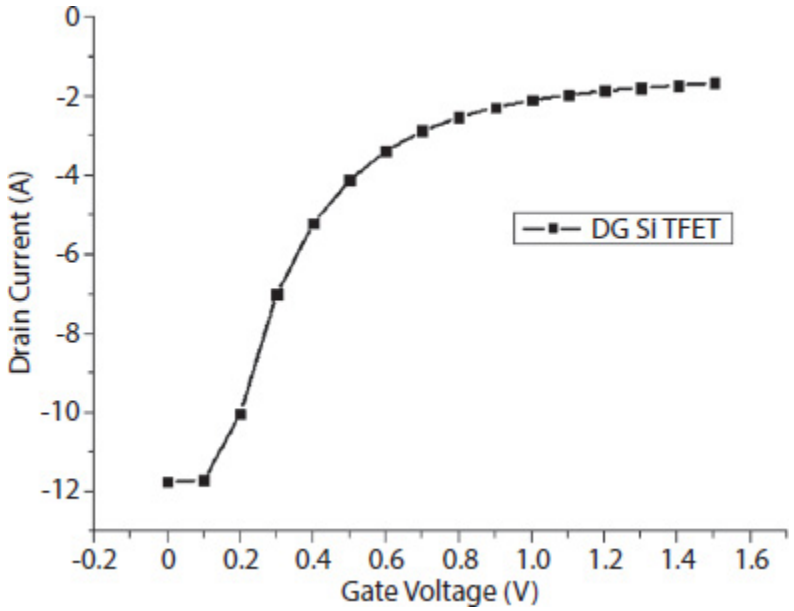

Figure 4.5 Drain current characteristics of silicon dual gate TFET.

4.3.2 Compact Models

An accurate compact model that detains the Trap Assisted Tunneling obtained from the surface traps is developed [5]. Considering Trap Assisted Tunneling has proven to obtain matching results with the experimental data for sub-threshold, an effective tunneling window based on the wavefunction following the Landauer-formalism- mechanism is derived.

4.4 Applications of Tunnel Field-Effect Transistor

4.4.1 TFET for Biosensor Applications

The world witnessed a deadly pandemic with COVID-19. As necessity is the starting point of any invention, biosensors are more substantial. Biosensors based on FET have gained popularity because of their accuracy of prediction, low power, and reduced cost [6]. MOSFETs yield quick results in a shorter duration of time, but short channel effects and its limitation of 60mV/decade sub-threshold swing will result in less device sensitivity and more dissipation of power as it is based on thermionic emission.

There is a focus towards a new device architecture called TFET that has device characteristics suitable for biosensors whose application varies from the medical field to the environmental monitoring field. Physiochemical reaction of biomolecules generates an electric signal captured by the biosensor device. TFET-based biosensor models [8] developed in different literature works are presented here.

TFET structure encompasses three regions: Source, Channel, and Drain. The main differentiating criteria between TFET and MOSFET is that source and drain doping are opposite: P+ doping is used for the source and N+ doping for the drain, as shown in Figure 4.6. The TFET-based biosensor portrayed shows the channel between the source and the drain contains a bio-recognition element. This element senses the bio-molecules and changes the concentration of charge at the channel surface. This will eventually lead to increased drain current as there is a reduction in tunneling length.

Improved response time and sensitivity are observed in a single silicon Nanowire based TFET biosensor whose structure is shown in Figure 4.7a. The TFET structure is in the electrolytic solution along with a controlled

gate. On the intrinsic channel region, a thin oxide layer is laid out as a receptor. Noise and reliability are the issues to be considered.

The structure used in a di-electric modulated biosensor TFET makes use of the concept of dielectric modulation for bio-sensing. The structure has a cavity region where the bio-molecules are made to reside. This cavity can be created in an oxide layer below the electrode of the gate. Once the biomolecules start to interact, the dielectric of the oxide layer changes, leading to effective coupling between the gate and dielectric. This leads to a change in band bending of energy levels, indicating a change in the drain current.

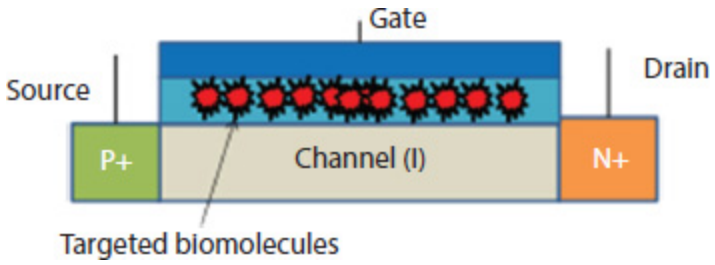

Figure 4.6 2D structure of TFET with targeted biomolecules [7].

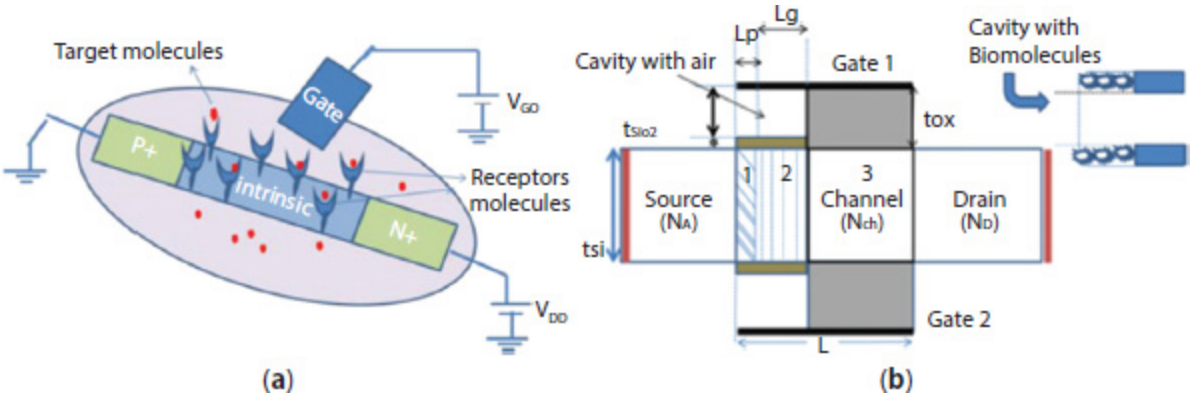

Figure 4.7 Schematic of (a) silicon nanowire-based TFET biosensor [10]; (b) dielectrically modulated TFET [9].

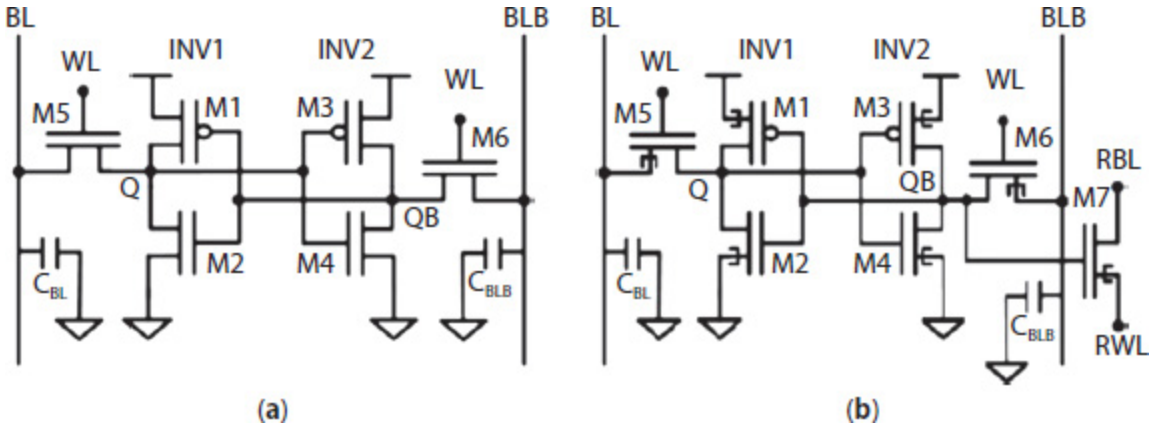

Figure 4.8 Structure of (a) 6T SRAM and (b) 7T SRAM [11].

4.4.2 TFET-Based Memory Devices

In sub-nanometer technologies, leakage power consumption is a major issue for memory devices. The fastest memory in the processor is Cache, where a higher percentage is occupied by Static Random Access Memory (SRAM), so most of the power is consumed by the memory device.

Analysis of 6T SRAM and 7T SRAM as depicted in the Figure 4.8 shows an improvement in the Noise Margin's Read and Write, respectively. The higher noise margins and reduced dissipation of power make TFET a better candidate to replace MOSFET for application in memory devices. Calculation of the read noise margin is made by the monitoring voltage transfer characteristic where DC voltage is swept at node Q and checking the voltage at node QB. The minimum bit line voltages required to change the node of the cells is defined as the Write Noise Margin.

4.4.3 TFETs for Mixed Signal Applications

The linkage of analog and digital systems has increased the essence of low-power mixed signal systems that are significantly efficient. The Internet of Things (IoT) is continuously emitting data in realtime that needs to be filtered after digitizing. Mixed signal systems are characterized by power, performance, and area, which are paramount requirements. A lot of researchers are spending ample time creating power-efficient and high-speed architectures for mixed-signals as shown in the Figure 4.9. Lower ON current and high ambipolarity hinders the application of TFET in mixed

signal processing, but it can be managed by proper usage of III–V band gap materials that are low and high at source and drain channel regions.

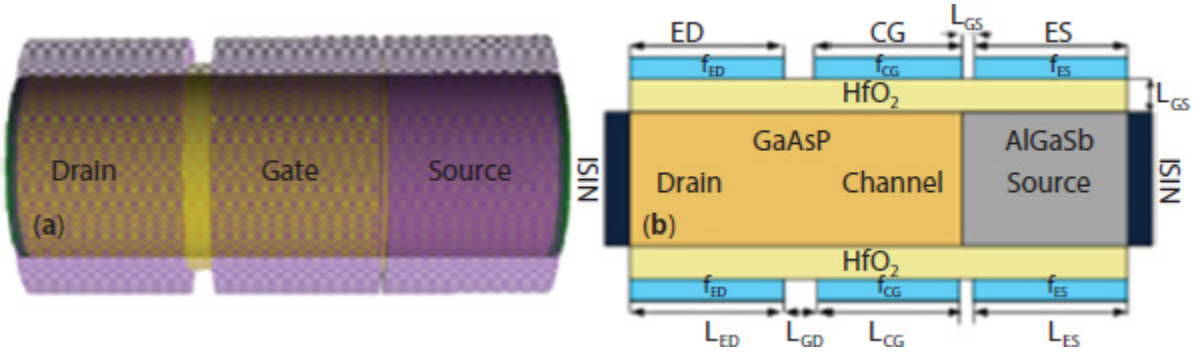

Figure 4.9 3D and 2D structure of AlGaSb/GaAsP electrically doped TFET [12].

High I_{ON}/I_{OFF} and lesser ambipolar are observed in AlGaSb/GaAsP Electrically Doped TFET. It is observed that the cut-off frequency is 1.4THz. It exhibits good linearity compared to other materials.

4.4.4 TFETs for Analog/RF Applications

Modifications in device structure and materials are yielding higher ON currents with suppressed ambipolarity. This behavior is useful for the TFET to be operated for analog/RF applications. Figures of merit, namely transconductance, cut-off frequency, and capacitances, are highly encouraging. Transconductance has shown superior performance when compared to other Field Effect Transistors. Transconductance in conjunction with total gate capacitance defines the cut-off frequency [13]. The total capacitance is illustrated by the following equation: Cgg=Cgd+Cgs. A major role is played by the gate to drain capacitance and is also inclined on the material used. Figure 4.10 shows cut-off frequency variation with that of gate voltage.

4.4.5 TFETs for Low-Power Applications

With the scaling down of the technology node from the nano-meter regime to the sub-nano-meter, many device structures are proposed to overcome the short channel effects and lower ON current observed in TFETs. The three-dimensional channel structures introduced for overcoming these shortcomings are FinTFET and Gate All Around TFET (GAA TFET).

Around 11mV/decade, the sub-threshold swing was reported to induce Fin technology to TFETs [14].

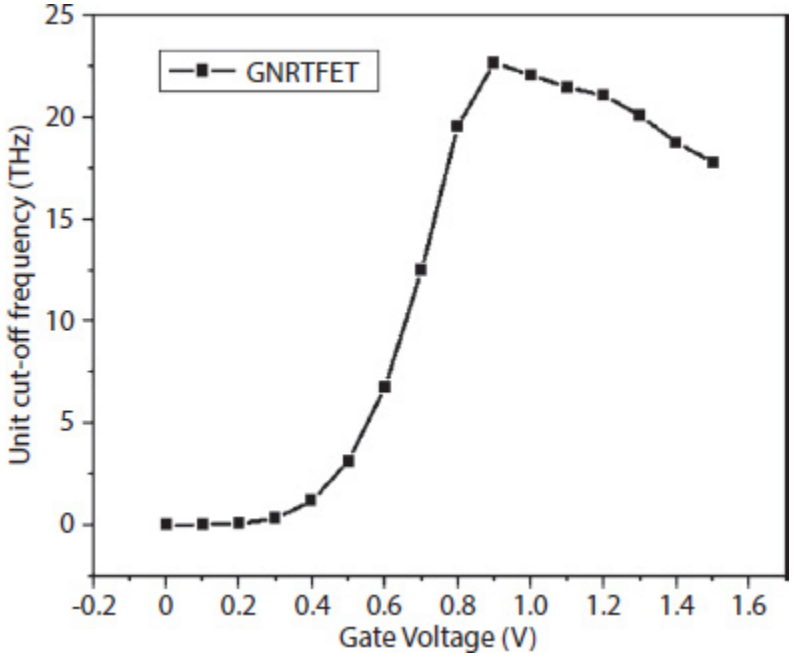

Figure 4.10 Frequency (cut-off) vs. gate voltage in TFET.

The addition of a channel in GAA TFET has resulted in increased ON current and decreased ambipolarity [15].

4.5 Road Ahead for Tunnel Field Effect Transistors

Even though TFETs have a sub-threshold swing lower than 60mV/decade and other excellent attributes to be used in low-power devices, the major challenge is to deliver higher ON current. Based on the results obtained by the researchers, it is optimistic that the problem of lower ON current can be resolved by choosing the materials for the device architecture. Still, higher optimization of the device and process have yet to be carried out.

Shifting from one process technology to another is critical from technology and financial perspectives. The cost invested will be fruitful only when TFETs will be able to surpass MOSFETs having higher gain and performance.

TFETs needs to deliver reduced sub-threshold swing even at a channel length of 10nm and below, so the impact of TFETs at lower process nodes, random fluctuations of doping, and reliability issues need to be taken care of.

In spite of all the pros and cons, TFETs are emerging as the next promising device that can outperform MOSFETs.

References

1. Abdurrahman Özgür Polat, Mutlu Avcı, Modified GRNN based atomic modeling approach for nanoscale devices and TFET implementation, Materials Today Communications, Volume 27,2021,102294,ISSN 2352-4928, https://doi.org/10.1016/j.mtcomm.2021.102294.

2. S. Markov, B. Aradi, C. Yam, H. Xie, T. Frauenheim and G. Chen, “Atomic Level Modeling of Extremely Thin Silicon-on-Insulator MOSFETs Including the Silicon Dioxide: Electronic Structure,” in IEEE Transactions on Electron Devices, vol. 62, no. 3, pp. 696-704, March 2015, doi: 10.1109/ TED.2014.2387288

3. Mamidala Jagadesh Kumar, Rajat Vishnoi and Pratyush Pandey, Tunnel Field-effect Transistors (TFET): Modelling and Simulation , Wiley UK, 250 pages, ISBN: 978-1-119-24629-9, November 2016.

4. Sneh Saurabh and Mamidala Jagadesh Kumar, Fundamentals of Tunnel Field Effect Transistors , CRC Press (Taylor & Francis), 300 Pages - 110 B/W Illustrations, ISBN 9781498767132, November 2016

5. R. N. Sajjad and D. Antoniadis, “A compact model for tunnel FET for all operation regimes including trap assisted tunneling,” 2016 74th Annual Device Research Conference (DRC), 2016, pp. 1-2, doi: 10.1109/DRC.2016.7548414.

6. Vigneshvar S., Sudhakumari C. C., Senthilkumaran Balasubramanian, Prakash Hridayesh,” Recent Advances in Biosensor Technology for Potential Applications – An Overview “,Frontiers in Bioengineering and Biotechnology, volume 4,2016.

7. Reddy NN, Panda DK. A Comprehensive Review on Tunnel Field-Effect Transistor (TFET) Based Biosensors: Recent Advances and Future Prospects on Device Structure and Sensitivity. Silicon. 2021;13(9):3085–100. Doi: 10.1007/s12633-020-00657-1. Epub 2020 Aug 26. PMCID: PMC7447593.

8. Sarkar D, Banerjee K (2012) Proposal for tunnel-field-effect transistor as ultra-sensitive and label-free biosensors. Appl PhysLett 100(14):143108

9. Narang R, Saxena M, Gupta RS, Gupta M (2012) Dielectric modulated tunnel field-effect transistor-a biomolecule sensor. IEEE Electron Device Lett 33(2):266–268

10. Gao A, Lu N, Wang Y, Li T (2016) Robust ultrasensitive tunneling-FET bio-sensor for point-of-care diagnostics. Sci Rep 6:22554

11. J. Singh, K. Ramakrishnan, S. Mookerjea, S. Datta, N. Vijaykrishnan and D. Pradhan, “A novel Si-Tunnel FET based SRAM design for ultra low-power 0.3V VDD applications,” 2010 15th Asia and South Pacific Design Automation Conference (ASP-DAC), 2010, pp. 181-186, doi: 10.1109/ ASPDAC.2010.5419897

12. Rajan, Chithraja & Samajdar, Dip & Lodhi, Anil. (2021). Investigation of DC, RF and Linearity Performances of III–V Semiconductor-Based Electrically Doped TFET for Mixed Signal Applications. Journal of Electronic Materials. 50. 10.1007/s11664-021-08753-7.

13. G.H. Nayana, P. Vimala, M. Karthigai Pandian, T.S. Arun Samuel. “Simulation insights of a new dual gate graphene nano-ribbon tunnel field-effect transistors for THz applications”, Diamond and Related Materials, 2021

14. Hemanjaneyulu K, Shrivastava M (2015) Fin enabled area scaled tunnel FET. IEEE Trans Electron Devices 62:3184–3191. https://doi.org/10.1109/TED.2015.2469678

15. Ravindran A, George A, Praveen CS, Kuruvilla N (2017) Gate all around nanowire TFET with high ON/OFF current ratio. Mater Today Proc 4:10637–10642. https://doi.org/10.1016/j.matpr.2017.06.434

Note

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5
Analysis of Channel Doping Variation on Transfer Characteristics to High Frequency Performance of F-TFET

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Abstract

In this chapter, an ultra-thin finger-like source-based Tunnel FET (F-TFET) is demonstrated for the impact of a change in channel doping level (N_C). The change in N_C may significantly affect the tunneling rate at the source-channel and drain-channel interface (SCI_{int} and DCI_{int}). Along with this, the energy band alignment and carrier injection process vary accordingly. Because of this, considerable change in ON state current (I_{ON}), OFF current (I_{OFF}), and ambipolar current (I_{ambi}) can be observed. The high range of N_C helps to limit the carrier movement and leads to mobility saturation at the source-channel interface. On the other hand, for highly doped sources and moderately doped drain regions, it advances the carrier injection. As a result, I_{ON} has opposing functionalities for increasing the doping level of the channel region. Along with this, the selection of models during the simulation process also affects the electrical performance of the TFET device. According to the N_C variation, the electric field also varies accordingly. Consequently, the SRH and TAT models' current functionalities show their significance according to the electric field because they are very susceptible to electric field variations. The BTBT model aspect dominates drain current under high E_{fields}. Hence, the change in N_C affects the device's effectiveness in areas such as analog and high-frequency functionality. This work performed a thorough study to ensure analog/RF performance and the reliability of F-TFET. With the help of the 2D-TCAD SILVACO tool, comprehensive analyses were carried out to investigate device sensitivity towards N_C variation with consideration to

necessary models. Moreover, a reliability investigation is established which reveals that N_C variation is unfavourable for the SS, ambipolar current, and I_{ON}/I_{OFF} ratio.

***Keywords*:** Electric Field (E_{fields}), Ambipolar, BTBT (Band-To-Band-Tunneling), Channel Doping (N_C)

5.1 Introduction

In distinctive bulk silicon, it becomes exceedingly challenging to devise abrupt metallurgical p-n contacts and mitigate SCEs (Short-Channel-Effects) as the physical gate length of MOSFETs downscales to the realm of nm in size. Double Gate MOSFET technology has become the most scalable of all MOSFET designs due to its outstanding management of SCEs, which is caused by the close interaction between the gates and the channel [1-4]. Because of this, MOSFET has had complete control over semiconductor devices in recent decades. To replace MOSFETs, TFETs have gained a lot of attention due to their ability to achieve subthreshold swings (SS) below 60 mV/decade at ambient temperature and enable further supply voltage reduction without compromising OFF-current [5, 6].

For device downscaling, DG-TFET with intrinsic channels are the ideal option since they provide benefits like a lack of the dopant fluctuation effect, which can cause variations in the threshold voltage, and drive current increased carrier mobility because there aren't any depletion charges to add to the effective electric field and reduce the mobility [7-9]. Moreover, because body doping is not a significant means for adjusting the threshold voltage, intrinsic channel TFET must fixate on gate work functions to accomplish specific threshold voltages on an integrated circuit [10].

In this chapter, we present a simulated finger-like source inserted within the channel with a single gate TFET (F-TFET) and analyse the outcomes for different values of N_C (ranging from 10^{14} cm^{-3} to 10^{18} cm^{-3}). The F-TFET comprises of an enhanced source-channel interface which is reflected in terms of higher I_{ON}. On the other side, the drain-channel interface is limited and direct tunneling between the source and drain is difficult, which will help minimize ambipolar conduction. The energy band diagram, E_{fields}, and

analog-RF parameters are used to analyse the device performance with drain current and ambipolar conduction. This device is a viable candidate for use as a low power device due to improved DC/analog and high frequency FOMs (figure of merits).

5.2 Simulated Device Structure and Parameters

The designed F-TFET is presented in Figure 5.1 (structure has a finger-like ultra-thin source region within the channel region) and includes multiple colours and physical characteristics. $Si_{0.5}Ge_{0.5}$ alloy is used in the highly Boron-dopant (P-type, $10^{20}cm^{-3}$) prepared source region. Si is used for the drain (Arsenic-dopant, $5x10^{18}cm^{-3}$) and channel (doping variation from 10^{14} to $10^{18}cm^{-3}$) materials with 1nm HfO_2 as the gate oxide. The t_S and L_S (thickness and length of source) are set to 3 nm and 35 nm, making the gate more easily controllable for both vertical and lateral tunneling between the source and gate region. The lateral tunneling length (L_t) is set to 4 nm. The other device proportions are as follows: t_d = 5 nm, L_g = 20 nm, $t_g = (2t_{cu} + t_s)$ = 30 nm, $t_{cb} = (t_d + t_{ox})$ = 6 nm, gate work function= 4.50 eV, total length of the device $L_{total} = (L_{cb} + L_d)$ = (60nm + 35nm) = 95 nm, and total height of the device $H_{total} = (t_{cb} + t_g)$ = (6 nm + 30nm) = 36 nm. The SILVACO ATLAS tool was used for all simulation experiments. The non-local BTBT framework supports the quantum tunnelling characteristic by identifying quantum tunnelling areas (qt regions) at the SCI_{int} and DCI_{int}.

5.3 DC Characteristics

Variations in fundamental DC FOMs, such as the EBDs (Energy Band Diagrams), I_{ds}-V_{gs} (Transfer Characteristics), V_{th} (threshold voltage), potential, recombination rate, E_{fields}, and Sub-threshold Swing (SS), are an acceptable approach for examining the initial stage of the device's vulnerability study under diverse channel doping levels [11, 12]. As a result, the effect of increasing N_C on the DC efficacy of F-TFET is extensively deliberated in this work. When N_C increases from 10^{14} cm^{-3}, a high number of empty states are generated within the channel region

because increasing dopants create empty states in the band gap [13]. These empty states have small ionisation energy and when further doping increases, dopants may create a band. Depending on the location of the generated band, the band gap will either increase or decrease. The intrinsic (n_i) and impurity (N_a) concentration are proportionately related to each other, as given by Equation 5.1. Due to high N_C, a high carrier concentration is present within the channel region [14-16].

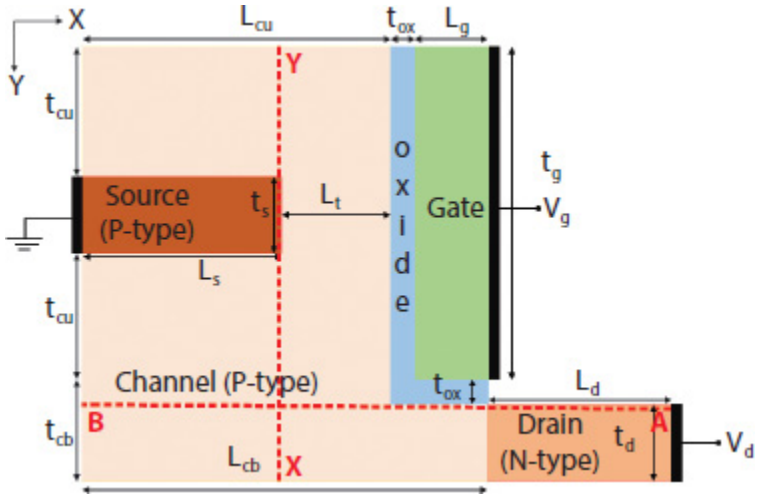

Figure 5.1 2D cross-sectional representation of F-TFET with two cut-lines: AB and XY.

$$n_i = N_a exp\left(\frac{E_g}{2kT}\right) \quad (5.1)$$

The doping profile of the source region is very high (10^{20} cm^{-3}) compared to the channel region. From Figure 5.2a, when N_C = 10^{14} and 10^{15} cm^{-3}, the band alignment is significantly improved at SCI_{int} and after that, the present potential barrier between bands increases because the higher doping of the channel leads to mobility degradation. A similar effect can be seen at the DCI_{int} in Figure 5.2b. The energy band alignment at both interfaces starts diminishing when N_C is higher than 10^{16} cm^{-3}.

The mobility and doping density are inversely related to each other and for an increasing doping profile, the mobility of charge carriers is diminished. Because of the reduced mobility, the movements of the charge carriers become restricted [17, 18]. This restricted movement turns into vibration

with further increases in doping level and it becomes zero for ideal conditions. As a result, the considered energy between the two points lessens and the potential at SCI_{int} and DCI_{int} started to decline with rising N_C in ON state conditions, as shown for SCI_{int} and DCI_{int} in Figures 5.3a and b, respectively.

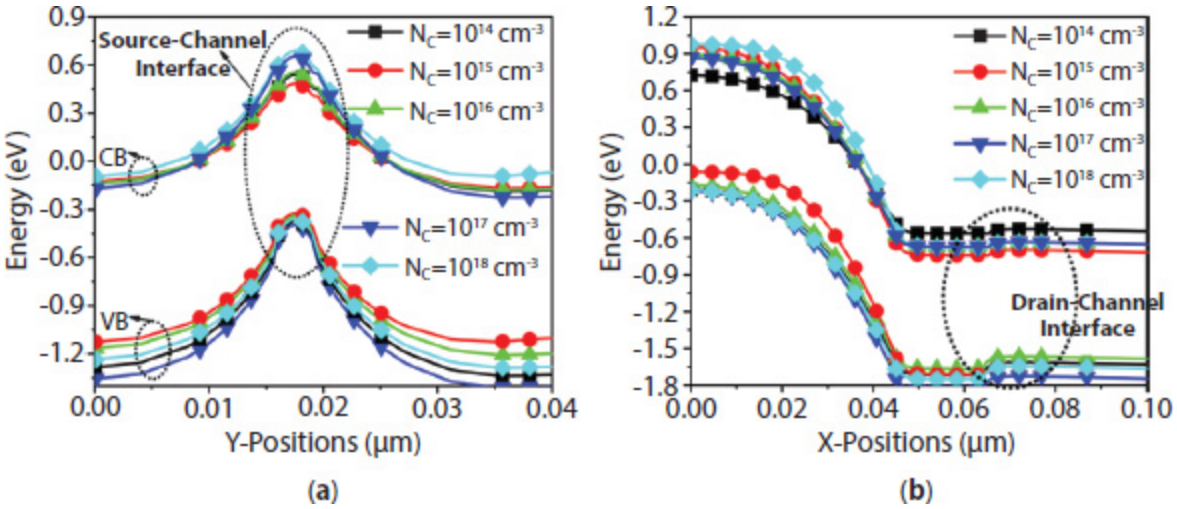

Figure 5.2 ON-state EBD at (a) Source-Channel-Interface (SCI_{int}) along XY cut-line and (b) Drain-Channel-Interface (DCI_{int}) along AB cut-line for various N_C.

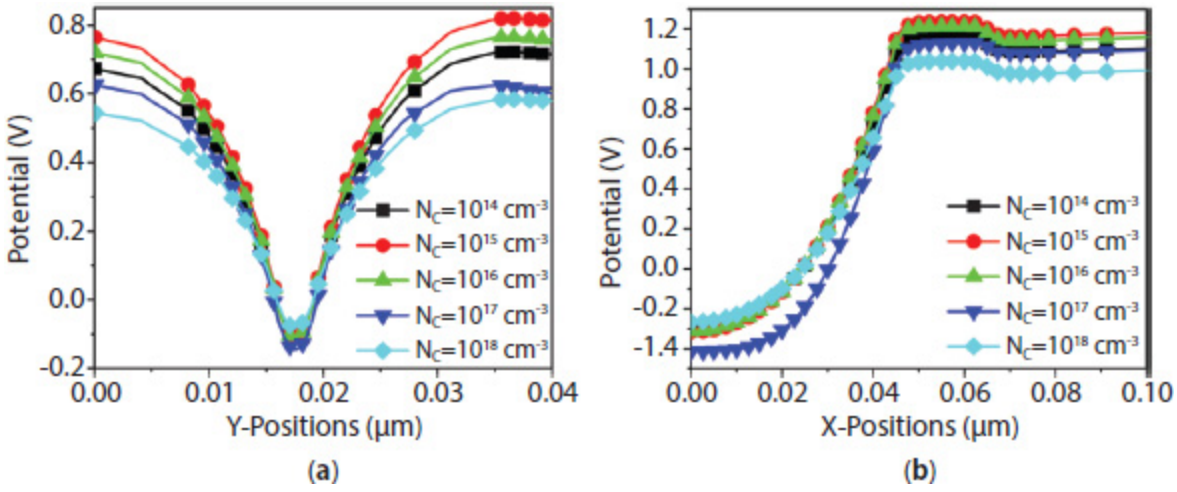

Figure 5.3 Ramifications of N_C on potential at (a) SCI_{int} and (b) DCI_{int}.

The E_{fields} at both interfaces are also significantly affected by the change in N_C because E_{fields} mainly depend on the carrier concentration and presented

force between them and both change with N_C for the F-TFET. The deviation in E_{fields} at SCI_{int} and DCI_{int} portrayed in Figures 5.4a and b. The E_{fields} start improving when N_C varies from 10^{14} to 10^{15} cm^{-3} and after that it starts decreasing because of the deduced potential between the charge carriers. When N_C= $10^{15}cm^{-3}$, E_{fields} = 3.01 x 10^6 V/cm (at SCI_{int}) and E_{fields} = 6.12 x 10^5 V/cm (at DCI_{int}).

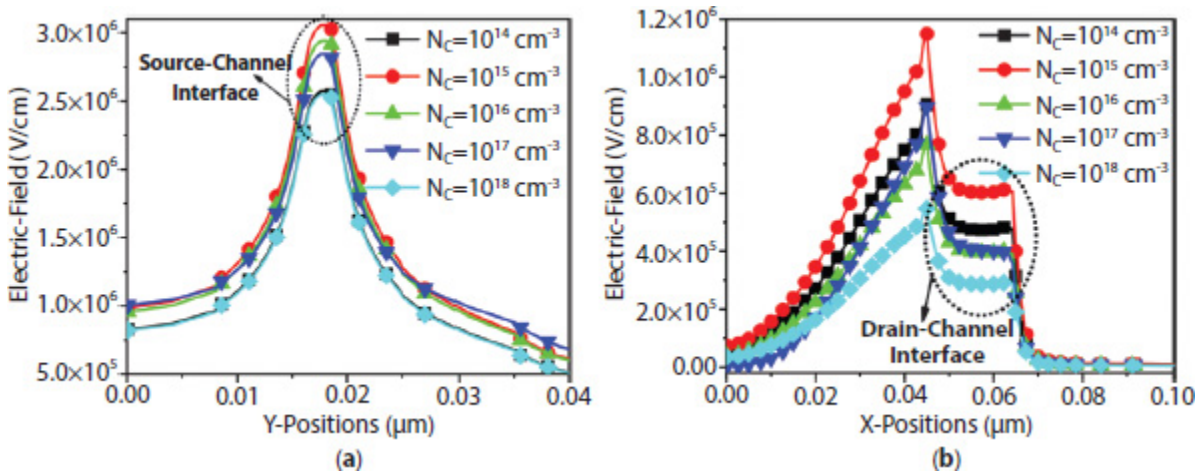

Figure 5.4 Variations in Electric Field (E_{fields}) for ON State at (a) SCI_{int} and (b) DCI_{int}.

The high E_{fields} at SCI_{int} helps increase I_{ON} and it is beneficial for improvements in device performance. E_{fields} at DCI_{int} try to increase the leakage/ ambipolar current of the device, which is not desirable for optimum device efficacy [19, 20]. The E_{fields} and potential significantly affect the generation and recombination rate of charge carriers at both interfaces. For an ideal case, generation and recombination at thermal equilibrium conditions are equal to each other. When an external supply is applied to the device, the equilibrium condition is disturbed and the recombination rate may be different from the generation rate [21, 22]. When N_C increases, a greater number of charge carriers are generated and ready to recombine with carriers present at either the source or drain region. Because of this, the recombination rate at SCI_{int} and DCI_{int} is enhanced as N_C increases from 10^{14} to 10^{18} cm^{-3}, as depicted in Figure 5.5a and b.

The drain current is not dependent on the channel doping profile; it depends on the source doping level. Since most charge carriers contained in the source rely on the proportional modification of charge carriers that tunnel from source to channel, the I_{ON} (saturated I_{ds}) is not purposefully changed by the N_C variation. The predominant majority charge carriers' (carriers of the source region which contributed to I_{ON} deviations) fractional modulation is not very noteworthy. But, when carrier density within the channel region changes because of doping concentration, the I_{ON} significantly varies with this. As a possible consequence, as can be shown in Figure 5.6, there was a noticeable N_C influence on the I_{ON} of the F-TFET. The maximum I_{ON} (1.08×10^{-4} A/μm) is achieved when N_C is set at 10^{15} cm^{-3}. The transfer characteristics of F-TFET are shown in Figure 5.6 on both a linear and semi-log axis.

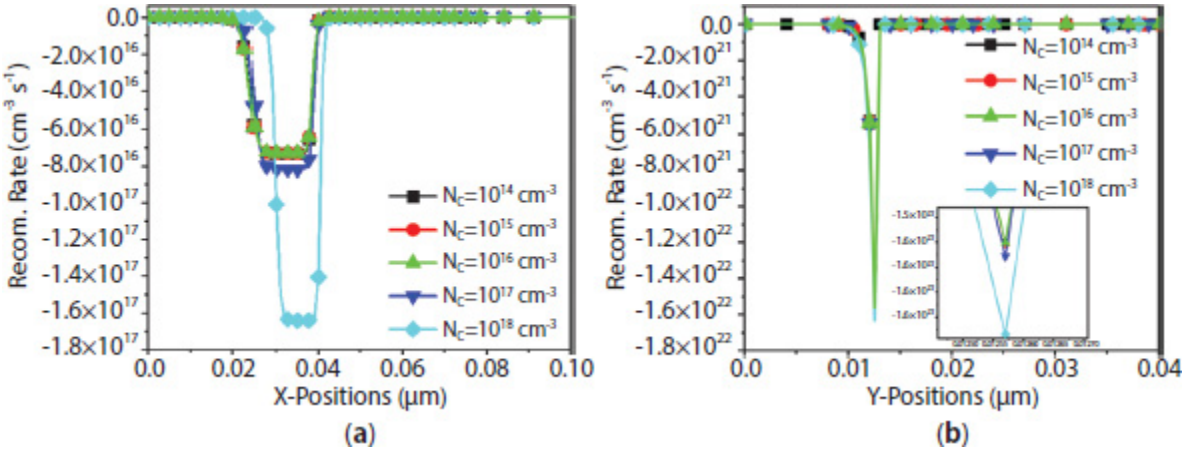

Figure 5.5 Variations in recombination rate for ON State at (a) SCI_{int} and (b) DCI_{int}.

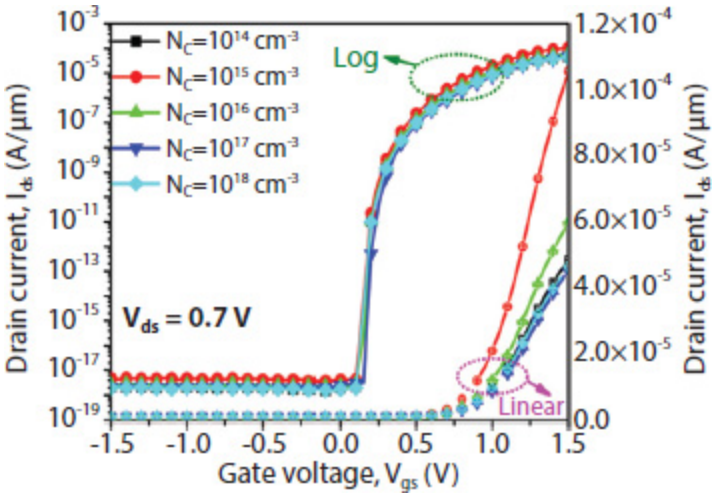

Figure 5.6 I_{ds}-V_{gs} plot to analyse the effect of channel doping deviations on transfer characteristics.

$$SS_{avg} = \frac{V_{th} - V_{off}}{\log\left(\frac{I_{th}}{I_{off}}\right)} \quad (5.2)$$

The implications of N_C on variation of ON-state current as well as I_{ON}/I_{OFF} ratio are depicted in Figure 5.7a. Since the higher I_{ON} of a simulated device is achieved for $N_C = 10^{15}$ cm^{-3} (Figure 5.7a, red plot) and the I_{OFF} is not significantly affected by the N_C deviations, the I_{ON}/I_{OFF} ratio significantly varies according to I_{ON}. The maximum I_{ON}/I_{OFF} ratio was achieved for the $N_C = 10^{15}$ cm^{-3} and the lowest for the $N_C = 10^{18}$ cm^{-3} (Figure 5.7a, yellow plot). The slope of the I_{ds}-V_{gs} plot in the subthreshold phase is inversely correlated to the SS value and its mathematical expression is given by Equation 5.2 [23]. Figure 5.7b shows that when N_C rises, the SS value rises (orange plot) and this is not acceptable for the switching speed of the investigated device. On either side, the suggested device's V_{th} increases (Figure 5.7b, black bar plot) as N_C increases, which is not favourable for applications requiring incredibly low power.

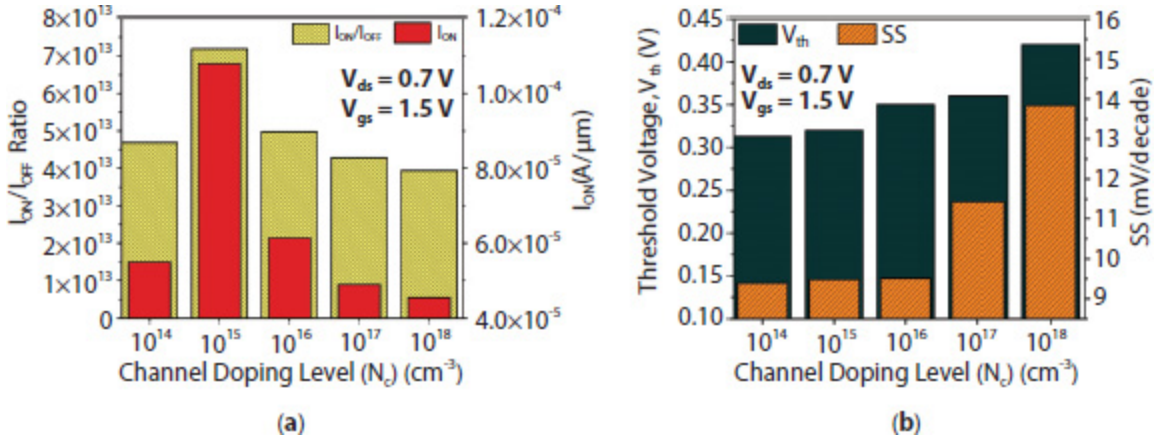

Figure 5.7 Variations in (a) I_{ON}/I_{OFF} Ratio (Left Y-axis) and I_{ON} (Right Y-axis); (b) V_{th} (Left Y-axis) and SS (Right Y-axis) for Different N_C.

5.4 Analysis of Analog/RF FOMs

Parasitic capacitances like gate-drain and gate-source capacitance (C_{gd} and C_{gs}), transconductance (g_m), maximum cut-off frequency (f_t), gain band with product (GBP), and a few other crucial characteristics examined in this investigation aim to explain the effects of N_C variations on the high efficiency of F-TFETs. A high I_{ON} with lower V_{th} and superior SS values usually plays a vital role for remarkable high-frequency performance of any FET device. Due to their simultaneous significance for parasitic oscillation across several frequency ranges, the C_{gd} and C_{gs} are essential to evaluating how well a device performs at high frequencies. For high-efficacy devices, C_{gd} and C_{gs} are being reviewed, but the parasitic capacitances must be as minimal as possible due to their effects on device speed which can result in a latency in the logical circuit [23, 24].

The increment in dopants within the channel region helps to exacerbate the inversion layer with the presence of charge carriers within the channel region. But, the significant change in the inversion layer cannot be seen as N_C increases, so the C_{gd} is not changed significantly, as displayed in Figure 5.8a. However, the presented potential barrier (reduced) at SCI_{int} varies according to the N_C (increase) values. Because of this, C_{gs} increases with increasing N_C, as described in Figure 5.8b.

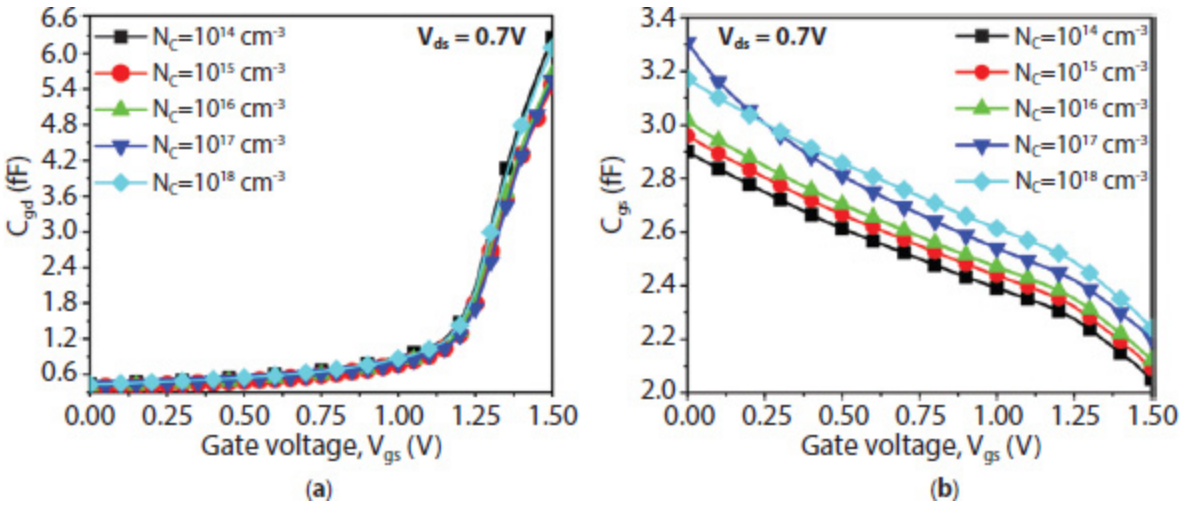

Figure 5.8 Plots of (a) C_{gd} and (b) C_{gs}.

The findings show that as V_{gs} increases from 0.0V to 1.50V, the F-TFET exhibits lower C_{gs} and C_{gd} at $N_C = 10^{15}$ cm^{-3} due to the increased carrier mobility across the channel and fewer inversion/accumulation processes at both interfaces.

To analyse the device speed and switching response, we need to examine the gm parameters of the device. The g_m is defined as the 1st derivative of I_{ds} to V_{gs} and it should be high for improved device performances [25]. The g_m curves for various N_C concentrations are shown in Figure 5.9a to make it more convenient to analyse amplification or analyse the current device ability of F-TFET. The maxima of the g_m plot are achieved for 10^{15} cm^{-3} doping of the channel region because the I_{ON} is higher. For other values of N_C, g_m start decreasing as N_C increased from 10^{15} to 10^{18} cm^{-3}. By determining the ratio of the g_m to $2\pi(C_{gd} + C_{gs})$, the value of the f_t can be obtained [26]. As shown in Figure 5.9b, the significantly larger g_m and lower $(C_{gd} + C_{gs})$ for the $N_C = 10^{15}$ cm^{-3} with high V_{gs} allows for the attainment of the improved figure of f_t.

GBP is adversely correlated with the device's C_{gd} value and linearly proportionate to the g_m. To achieve superior high frequency endurance, GBP must be large [27]. Although the g_m and C_{gd} both rise with N_C (10^{15} cm^{-3}), very high gm causes GBP to improve with low $N_C = 10^{15}$ cm^{-3} and

declines when $N_C > 10^{15}$ cm^{-3}. For N_C (10^{15} cm^{-3}), the percentage deviation of fluctuation in GBP is 4.56% (increase) with respect to $N_C > 10^{15}$ cm^{-3}. Transit time (τ), another crucial factor, is used to examine the device's response time and delay [28]. A considerable change in τ is seen when N_C varies and its minima (0.061 ms) achieved when N_C sis et to $10^{17}cm^{-3}$, as depicted in Figure 5.10b.

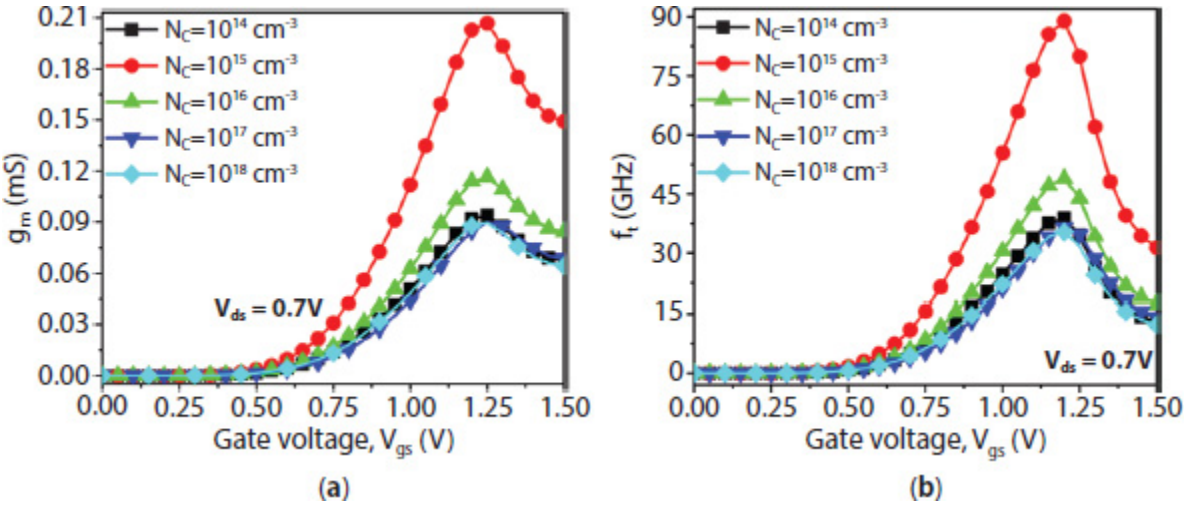

Figure 5.9 Curves of (a) g_m and (b) f_t under N_C deviations according to gate voltage.

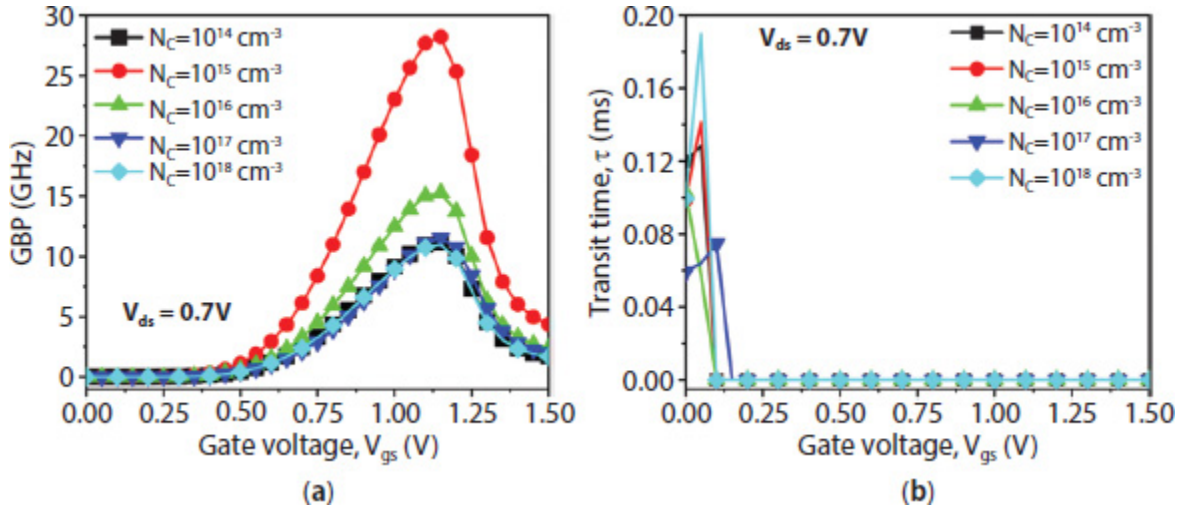

Figure 5.10 Variation in (a) GBP and (b) transit time.

The study of TFP and is important to demonstrate device efficacy, offset among power dissipation, and functioning bandwidth [26]. Figures 5.11a

and b exhibit the effects of distinct N_C values on TFP and TGF. TFP and TGF significantly decline with higher values of N_C, as the Vgs become high. For smaller Vgs, both the parameters increase and after attainting their maxima and start decreasing because of mobility saturation and the maximum cut-off frequency of the device being low (Figure 5.9b).

The overall deviation in the F-TFET performance parameters with changes in channel doping level is summarized in Table 5.1. From Table 5.1, we can clearly find the best suited doping level for the channel region of the simulated device structure. Along with this, we can also select the optimum frequency range within that device to work efficiently without any performance degradation.

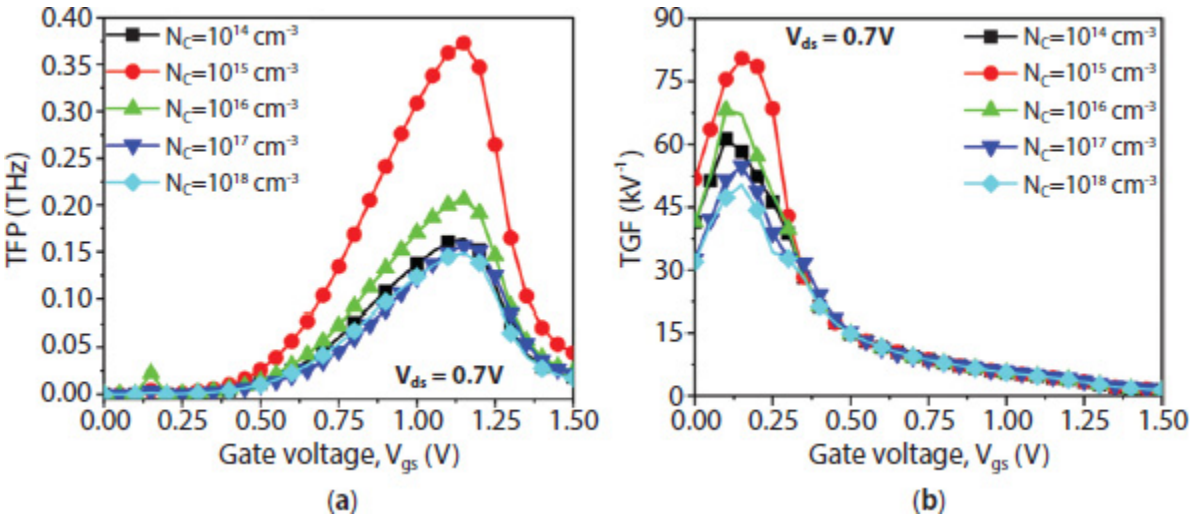

Figure 5.11 Variation in (a) TFP and (b) TGF.

Table 5.1 Overview of critical parameters for different doping levels of channel region.

Parameters	**Channel doping level (N^C)**				
	10^{14} cm^{-3}	**10^{15} cm^{-3}**	**10^{16} cm^{-3}**	**10^{17} cm^{-3}**	**10^{18} cm^{-3}**
I_{ON} (A/μm)	5.5×10^{-5}	1.08×10^{-4}	6.14×10^{-5}	4.89×10^{-5}	4.54×10^{-5}
I_{OFF} (A/μm)	1.17×10^{-18}	0.15×10^{-18}	2.33×10^{-18}	1.14×10^{-18}	1.15×10^{-18}
I_{ON}/I_{OFF}	4.68×10^{13}	7.18×10^{13}	4.98×10^{13}	4.28×10^{13}	3.94×10^{13}
I_{ambi} (A/μm)	2.17×10^{-18}	4.82×10^{-18}	2.63×10^{-18}	2.14×10^{-18}	2.00×10^{-18}
SS (mV/decade)	9.39	9.48	9.51	11.42	13.84
V_{th} (V)	0.313	0.32	0.35	0.36	0.42
C_{gd} (fF)	6.21	5.38	5.46	5.42	5.92
C_{gs} (fF)	2.05	2.092	2.18	2.25	2.34
g_m (*m*S)	0.081	0.208	0.118	0.091	0.86
f_t (GHz)	32.25	88.34	47.98	35.08	34.11
GBP (GHz)	12.84	27.89	16.21	14.56	13.02
TT (ms)	0.123	0.091	0.098	0.071	0.1001
TFP (THz)	0.18	0.38	0.201	0.173	0.168
TGF (kV^{-1})	42.05	51.21	43.1	33.81	33.53

5.5 Conclusion

In this chapter, the effect of channel doping on device efficacy is investigated to find the optimal N_C value. Improved SS and V_{th} values are observed if the N_C is set between 10^{15} and 10^{16} cm^{-3}. When compared to lower N_C, there is a corresponding drop in I_{ON}/I_{OFF} ratio as lower I_{ON} is achieved at higher N_C and ambipolar current is not affected much by N_C deviations. As the electric field and potential significantly decrease for increasing N_C, the overall device performance is also degraded with this. As

per consideration of outcomes, the peak value of I_{ON} (1.08×10^{-4} A/μm) and lower SS (9.48 mV/decade) with optimum V_{th} (0.32 V) are accomplished for $N_C = 10^{15}$ cm^{-3}. Additionally, the functionality of the F-TFET is examined while considering the cumulative effects of N_C on ON-state amenities and RF efficacy aspects. Capacitances, f_t, and GBP are significantly impacted by higher N_C, which lowers efficiency of the device in digital logic implementations. We found that RF limitations are more susceptible to higher N_C values, which does not allow us to assess the device's performance for high-frequency operations. The analysis suggests that the F-TFET might provide a viable option for enhanced analog/RF and ultra-low power applications when Nc is between 10^{15} and 10^{16} cm^{-3}.

References

1. S.-W. Sun, P.G. Tsui, Limitation of CMOS supply-voltage scaling by MOSFET threshold voltage variation. IEEE J. Solid-state Circuits 30(8), 947–949 (1995).

2. S.M. Turkane, A. Kureshi, Review of tunnel field-effect transistor (TFET). Int. J. Appl. Eng. Res. 11(7), 4922–4929 (2016)

3. Avci U. E, Morris D. H., Young I. A. (2015) Tunnel field-effect transistors: Prospects and challenges. IEEE J Electron Devices Soc 3(3):88–95

4. Singh P., Samajdar D. P., Yadav D. S. (2021) Doping and dopingless tunnel field effect transistor. In: 2021 6th International Conference for Convergence in Technology (I2CT), IEEE, pp 1–7.

5. W.Y. Choi, B.-G. Park, J.D. Lee, T.-J.K. Liu, Tunneling field effect transistors (tfets) with subthreshold swing (ss) less than 60 mv/dec. IEEE Electron Device Lett. 28(8), 743–745 (2007)

6. Kumar N., Raman A. (2020) Prospective sensing applications of novel heteromaterial based dopingless nanowire-tfet at low operating voltage. IEEE Trans Nanotechnol 19:527–534.

7. Prabhat Singh and D. S. Yadav, “Design and investigation of f-shaped tunnel fet with enhanced analog/rf parameters,” Silicon, pp. 1-16, 2021.

8. Yadav D. S., Sharma D., Agrawal R., Prajapati G., Tirkey S., Raad B. R., Bajaj V. (2017) Temperature based performance analysis of doping-less tunnel field effect transistor. In:2017 International Conference on Information, Communication, Instrumentation and Control (ICICIC), IEEE, pp 1–6.

9. Parmar N., Singh P., Samajdar D. P., Yadav D. S. (2021) Temperature impact on linearity and analog/rf performance metrics of a novel charge plasma tunnel fet. Appl Phys A 127(4):1–9

10. P.G. Der Agopian, M.D.V. Martino, S.G. dos Santos Filho, J.A. Martino, R. Rooyackers, D. Leonelli, C. Claeys, Temperature impact on the tunnel fet off-state current components, Solid-State Electron. 78, 141–146 (2012)

11. P. Singh and D. S. Yadav, \Impactful study of f-shaped tunnel fet,” Silicon, pp. 1-7, 2021.

12. Upasana M. G., Narang R., Saxena M. (2016) Impact of dielectric material and temperature variations on the performance of tfet with dielectric pocket. In: 2016 IEEE Annual India Conference (INDICON), IEEE, pp 1–4.

13. Tirkey S., Sharma D., Yadav D. S., Yadav S. (2017) Analysis of a novel metal implant junctionless tunnel fet for better dc and analog/rf electrostatic parameters. IEEE Trans Electron Devices 64(9):3943–3950.

14. Singh P., Samajdar D. P., Yadav D. S. (2021) A low power single gate l-shaped tfet for high frequency application. In: 2021 6th International Conference for Convergence in Technology (I2CT), IEEE, pp 1–6

15. S. B. Rahi, P. Asthana & S. Gupta, “Heterogate junctionless tunnel field-effect transistor: future of low-power devices”, Journal of Computational Electronics, vol. 16, issue.1 pp: 30-38,2017,IF:1.532,indexing:SCOPUS,SCI,ISSN:1569-8025. https://doi.org/10.1007/s10825-016-0936-9

16. Singh, P., Yadav, D.S. Assessing the Impact of Drain Underlap Perspective Approach to Investigate DC/RF to Linearity Behavior of L-Shaped TFET. Silicon (2022). https://doi.org/10.1007/s12633-022-01814-4

17. D. S. Yadav *et al.*, "A Comparative Study of GaP/SiGe Hetero Junction Double Gate Tunnel Field Effect Transistor," 2017 IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), 2017, pp. 195-199, doi: 10.1109/iNIS.2017.48.

18. S.B.Rahi, B. Ghosh and B. Bishnoi, "Temperature Effect on Hetero Structure Junctionless Tunnel FET", Journal of Semiconductors, vol.36, issue.3, pp: 034002_1-034002_5, 2015, indexing: Scopus, Web of Science. ISSN:2058-6140, https://doi.org/10.1088/1674-4926/36/3/034002

19. Kumar, S., Yadav, D.S. Assessment of Interface Trap Charges on Proposed TFET for Low Power High-Frequency Application. Silicon (2022). https://doi.org/10.1007/s12633-021-01616-0

20. P. Singh and D. S. Yadav, "Impact of tunneling length on analog/RF performance of L-shaped TFET," 2021 First International Conference on Advances in Computing and Future Communication Technologies (ICACFCT), 2021, pp. 114-118, doi: 10.1109/ICACFCT53978.2021.9837344.

21. Yadav, D.S., Kamal, M. Performance Analysis of Hetero Gate Oxide with Work Function Engineering Based SC-TFET with Impact of ITCs. Silicon (2022). https://doi.org/10.1007/s12633-022-01792-7

22. S.B. Rahi, B. Ghosh, "High-k Double Gate Junctionless Tunnel FET with Tunable Bandgap", RSC Advances, vol. 5, issue 67, pp-54544-54550, 2015, IF: 3.119, indexing: Web of Science. ISSN: 2046-2069, https://doi.org/10.1039/C5RA06954H

23. Singh, P., Yadav, D.S. Performance analysis of ITCs on analog/RF, linearity and reliability performance metrics of tunnel FET with ultra-thin source region. Appl. Phys. A 128, 612 (2022). https://doi.org/10.1007/s00339-022-05741-4

24. Yadav, D.S., Sharma, D., Tirkey, S., Sharma, D.G., Bajpai, S., Soni, D., Yadav, S., Aslam, M. and Sharma, N. (2018), Hetero-material CPTFET with high-frequency and linearity analysis for ultra-low power applications. Micro Nano Lett., 13: 1609-1614. https://doi.org/10.1049/mnl.2018.5075

25. Kumar N., Raman A. (2020) Low voltage charge-plasma based dopingless tunnel field effect transistor: analysis and optimization. Microsyst Technol 26(4):1343–1350.

26. Singh P., Yadav D. S. (2021) Impact of temperature on analog/rf, linearity and reliability performance metrics of tunnel fet with ultra-thin source region. Appl Phys A 127(9):1–15

27. Kamal M., Yadav D. S. (2021) Effects of linearity and reliability analysis for hgo-dw-sctfet with temperature variation for high frequency application. Silicon, pp 1–11.

28. D. Kumar, S.B. Rahi, P. Kuchhal “Investigation of Analog Parameters and Miller Capacitance affecting the Circuit Performance of Double Gate Tunnel Field Effect Transistors (TFETs)” Int. Conference on Intelligent Communication, Control and Devices, 2020. Indexing: Scopus (Springer).

Note

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6
Comparative Study of Gate Engineered TFETs and Optimization of Ferroelectric Heterogate TFET Structure

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Abstract

In this chapter, the electrical characteristics of various structures of TFET with gate engineering like conventional single gate TFET (Conv), Double gate TFET (DG), SOI TFET (SOI), Stack Gate TFET (Stack), and Heterogate TFET with Ferro gate (Hetero) have been studied. A new TFET structure based on the study of various architectures has been explored which incorporates the ferroelectric effect on a heterogate structure to overcome the limitations of TFETs and improve the ON current. Ferroelectric insulators show the property of negative capacitance which would amplify the applied gate voltage. This combination helps to achieve an improved I_{ON}/I_{OFF} ratio and lowered subthreshold swing (sub 60 mV/dec). Further, this will lead to nonvolatile high-density memory applications. A comprehensive study of electrical characteristics of the proposed device including short channel effects like the Drain Induced Barrier Lowering effect, Random Dopant fluctuation effect, study of interface traps charges on the gate semiconductor interface, and the impact of temperature on the proposed device transfer characteristics has been done. An additional dielectric layer is added to increase the memory window of the Ferro electric based Heterogate device. To extend the memory window through supplementary charges at the gate metal and ferroelectric interface, a portion of the injected charges are retained during the polarization switching, causing Coercive Voltage (Vcor) to rise, and thus, improving the Memory Window as well.

The simulation of the devices has been done with the Sentaurus TCAD tool. To validate the simulation results, physics-based analytical models are also proposed. Poisson-based models are developed for the proposed structure to observe the surface potential of the device

***Keywords*:** Tunnel FET, band-to-band tunnelling, heterogate, ferroelectric, surface potential, subthreshold swing, random dopant fluctuation, interface trap

6.1 Introduction

The TFET is said to be a prospective option as a future transistor owing to the low subthreshold swing and subsequently low supply voltage operation [1]. They operate in reverse-biased conditions. Reverse-bias conditions create the possibility of tunnelling and low OFF current. Tunnel FET has a low subthreshold swing but suffers from the drawback of low ON current when compared to MOSFET [2]. In order to come up with a unique switch with improved current in the ON state which overcomes the drawback of TFET, Salahuddin and Datta proposed that, by incorporating a ferroelectric (Fe) insulator in the insulator of a metal oxide field effect transistor gate stack, it can be observed that there is a possibility to execute a step-up voltage transformer as an effect of negative capacitance that can lead to high decrease in subthreshold swing due to amplification of the gate voltage [3]. This paper deals with the study of TFETs incorporating the ferroelectric effect. Si:HfO_2 is used as the ferroelectric material, as it is one of the most recent materials which shows ferroelectric properties even after being scaled down. The memory window of the proposed device has been increased by adding an extra dielectric layer. The chapter is organized as follows: Section 6.2 describes various comparisons of Tunnel FETs, Section 6.3 consists of the main device structure and the analytical model development, and Section 6.4 shows the validation of the model, study of electrical characteristics under various circumstances like trap, temperature, random dopant fluctuation, and in the presence of an additional dielectric layer. Finally, the chapter concludes and a reference section is also added at the end.

6.2 Study of Different TFET Structures

Initially, various structures of n type TFETs were studied in order to choose the most favorable base structure for applying the ferroelectric effect. The following structures were simulated:

1. Conventional TFET (Conv)
2. Double Gate TFET (DG)
3. SOI TFET (SOI)
4. Stack gate TFET (Stack)
5. Heterogate TFET (Hetero)

The Double Gate TFET has better control over the channel due to the presence of a double channel under the gates [4]. The SOI devices have various advantages like reduced latch up effect, less parasitic capacitance, and ease to make shallow junctions [5].

Stack gate has several advantages. The saturation of SiO_2 scaling has been forecasted since the late 80s. The growing gate leakage current results in the enhancement of direct tunneling current. To lessen this tunneling current, the physical thickness of the gate oxide has to be enlarged beyond the tunneling limit. The probable solution lies with the dielectric materials with dielectric constants higher than SiO_2 [6]. The high K gate dielectrics have several issues with the gate electrode contacts. So, gate stack structure have been introduced to mitigate several interface issues [7].

Heterogate is another promising option in the case of Tunnel FET structure in order to improve the ON current and reduce the ambipolar current [8]. Also, the ferroelectric effect was applied on conventional TFET to verify the effect of negative capacitance on lowering of Subthreshold Swing [9].

The lengths of Source, Channel, and Drain are 20nm, 30nm, and 20nm, respectively. The Source and Channel are doped with Boron with doping concentrations of $1\times10^{+20}$ cm^{-3} and $1\times10^{+15}$ cm^{-3}, respectively. The Drain is doped with Arsenic with a doping concentration of $1\times10^{+18}$ cm^{-3}. SiO_2 and HfO_2 thickness in the gate are of 2nm each. The Ferroelectric layer of Si:HfO_2 has a thickness of 15nm with a Silicon doping concentration of $1\times10^{+13}$ cm^{-3}.

6.2.1 Simulation Configuration

The results of electrical parameters of the devices have been obtained using Sentaurus TCAD (Technology Computer-Aided Design) [10]. It is a commercial TCAD tool from Synopsys. The structures have been constructed in the Sentaurus Structure Editor and the current characteristics have been observed in Sentaurus Visual and Sentaurus Inspect. An SDevice has been used to incorporate various physical models into the study. For calibrating the TCAD models, calibration has been done with experimental results. A bandgap narrowing model is included as high doping concentration carriers can tunnel through the narrow tunnel barrier. To account for the tunneling mechanism, the non-local band-to-band tunneling (BTBT) model enabling Fermi Dirac statistics is also incorporated. Further, the Shockley Read Hall recombination model is employed. Maxwell and Poisson equations are employed to calculate the surface potential. Temperature is specified in the Physics section in order to study the temperature dependency. The study of Traps, Acceptors, or Donor types, along with concentration, are specified in a Traps model in the physics section. In order to activate the ferroelectric model, the keyword Polarization in the Physics section is specified. Remanent polarisation, saturation polarisation, and coercive field values are mentioned in parameter files to characterize the properties of ferroelectric material [8].

6.2.2 Comparison of Electrical Parameters of Different Structures of TFET

The I_{ON}/I_{OFF} values and subthreshold swing values are depicted in Figure 6.1 and Figure 6.2, respectively.

The proposed structure for Ferroelectric Heterogate TFET has the least average SS and second-best I_{ON}/I_{OFF} after conventional ferroelectric TFET. This is due to an increase of I_{OFF} along with an increase in I_{ON} due to further narrowing of the tunneling barrier in a heterogate structure. The heterogate structure gives better gate control at the tunneling junction and provides reduced ambipolar current.

Observing the statistics, it can be inferred that applying the Ferroelectric effect on a Heterogate structure could combine the best I_{ON}/I_{OFF} with the

least subthreshold swing value. This is the motivation towards the structure proposed in this paper.

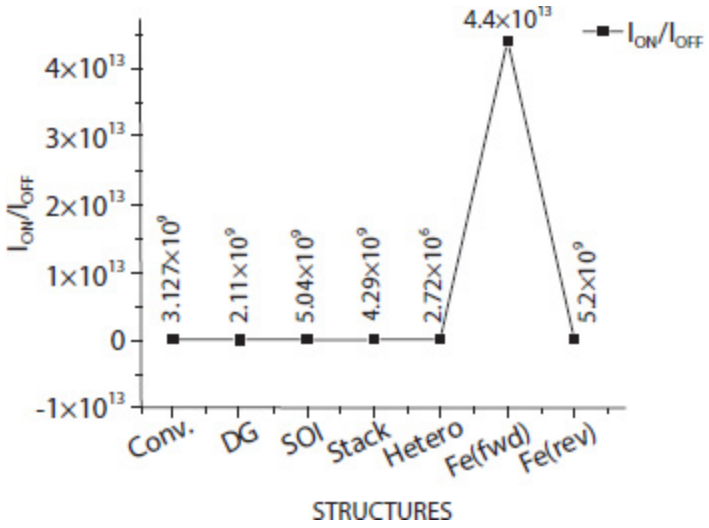

Figure 6.1 I_{ON}/I_{OFF} for different structures.

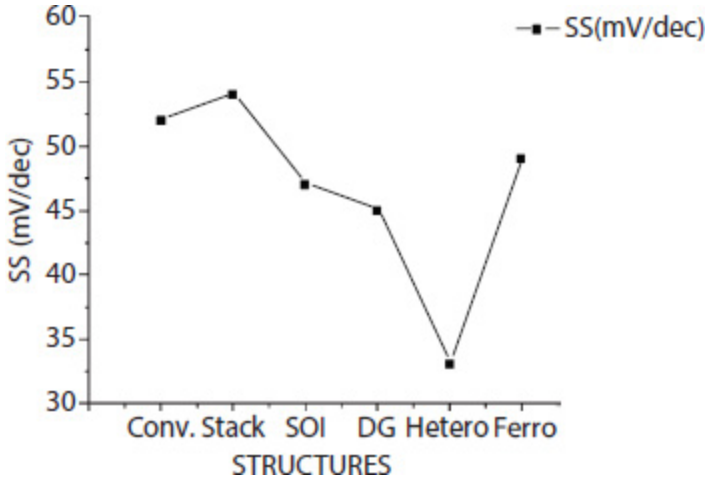

Figure 6.2 Least subthreshold swing value for different structures.

6.3 Proposed Structure

The Ferroelectric Heterogate TFET was first simulated using PolySilicon Gate contact and the FE layer was deposited using atomic layer Deposited Silicon doped HfO_2 film with 15nm thickness. As depicted in Figure 6.3, the flatband voltage needs to be increased in order to shift the curve towards the right and avoid high OFF current. This was done using Silver as a gate contact because the work function of Silver is higher than that of

PolySilicon, as shown in the equation below. Also, the gate dimensions could be scaled down by lowering the thickness of $Si:HfO_2$ to 5nm.

Flatband Voltage is given by:

$$V_{FB} = \phi_{MS} - \frac{Q'_o}{C'_{ox}}$$

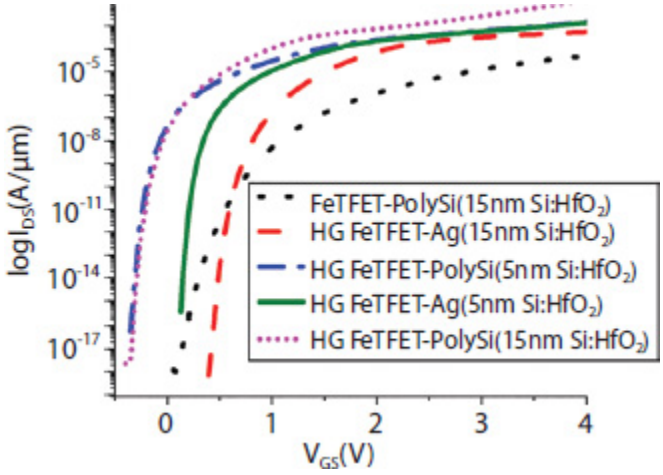

Figure 6.3 I_D vs. V_{GS} for various ferroelectric structures.

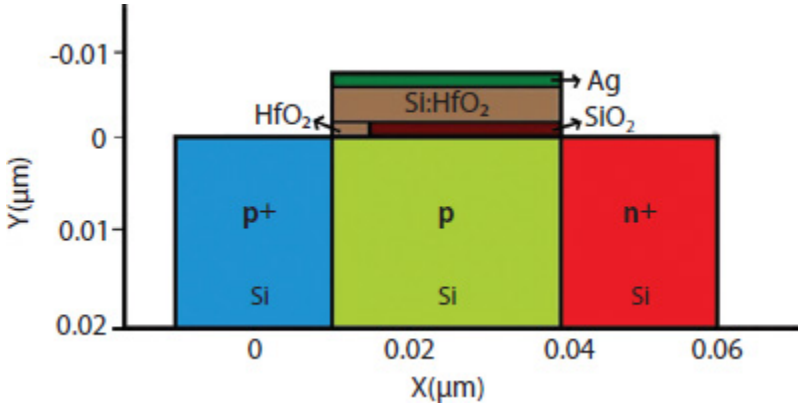

Figure 6.4 Heterogate ferroelectric tunnel field effect transistor (HF TFET).

where $\phi_{MS} = \phi_M - \phi_S$

As $\phi_{Ag} > \phi_{polySi}$, the flatband voltage is increased and higher gate voltage is needed to turn on the device.

Hence, the final proposed structure is given in Figure 6.4.

6.4 Results and Discussion

6.4.1 2-D Model for Surface Potential

The device structure is shown in Figure 6.5 and distinct regions are shown in order to develop a mathematical model. For formulating the Poisson equation-based physical model, the device is divided into four regions.

In regions 1, 2, 3, and 4 in Figure 6.5, the 2-D Poisson's equation is as follows [9]:

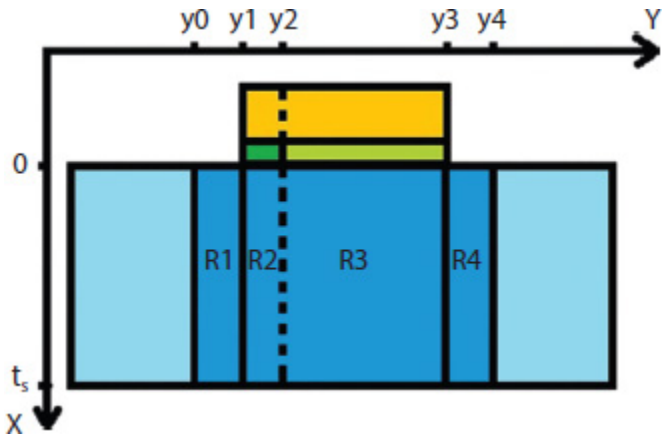

Figure 6.5 Heterogate TFET-1.

$$\frac{d^2\psi(x,y)}{dx^2}+\frac{d^2\psi(x,y)}{dy^2}=-\frac{qN_i}{\epsilon_s} \tag{6.1}$$

Here, ψ (*x*, *y*) is the 2-D potential, $\in_s$ is the permittivity of Silicon in the four regions, and N is the doping concentration in each region.

The potential balance equation for this structure can be written as follows [11]:

$$V_{gs}-\psi_s-V_{FB}-V_{fe}-\psi_{ox}=0 \tag{6.2}$$

$$V_{gs}=\psi_s+V_{FB}+2\alpha t_f\varepsilon_{Si}\frac{d\psi(0,y)}{dx}+\frac{\varepsilon_{Si}}{C_{oxi}}\frac{d\psi(0,y)}{dx} \tag{6.3}$$

In the above equation, voltage across ferroelectric material is given by Landau's theory [12] and the following equation [11]:

$$V_{fe} = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5$$

The surface potential can be approximated as a parabolic function [13]. Hence, we have adopted the following equation for 2-D potential:

$$\psi(x, y) = a_0(y) + a_1(y)\, x + a_2(y)\, x^2 \tag{6.4}$$

At x=0,

$$\psi(0, y) = \psi_s(y).$$

From equation (6.3), we get the electric field equation as follows:

$$E_x(0,y) = \frac{d\psi(0,y)}{dx} = \frac{V_{gs} - \psi_s - V_{FB}}{2\alpha t_f \varepsilon_{Si} + \frac{\varepsilon_{Si}}{C_{oxi}}} \tag{6.5}$$

At $x = t_s$,

$$\psi(x,y) = a_0(y) + a_1(y)t_s + a_2(y)t_s^2 \tag{6.6}$$

Applying (6.5) and (6.6) in (6.4), we get

$$a_0(y) = \psi_s(y) \tag{6.7}$$

$$a_1(y) = \frac{V_{gs} - \psi_s(y) - V_{FB}}{2\alpha t_f \varepsilon_{Si} + \frac{\varepsilon_{Si}}{C_{oxi}}}$$

$$a_2(y) = -\frac{a_0(y) + a_1(y)t_s}{t_s^2}$$

Thus, we get the surface potential as:

$$\psi(x,y)=\psi_s(y)+\frac{V_{gs}-\psi_s(y)-V_{FB}}{2\alpha t_f\varepsilon_{Si}+\frac{\varepsilon_{Si}}{C_{oxi}}}x+$$

$$\left(\frac{\psi_s}{t_s^2}+\frac{1}{t_s}\frac{V_{gs}-\psi_s(y)-V_{FB}}{2\alpha t_f\varepsilon_{Si}+\frac{\varepsilon_{Si}}{C_{oxi}}}\right)x^2$$

Double differentiating the above expression with respect to x and y and substituting in (6.1),

$$\frac{d^2\psi(x,y)}{dx^2}+\frac{d^2\psi(x,y)}{dy^2}=-\frac{qN_i}{\epsilon_s}$$

$$\left(-\frac{2}{t_s^2}+U_i\right)\psi_s(y)+\psi_s''(y)=U_i(V_{gs}-V_{FB})-\frac{qN_i}{\epsilon_s}$$

where $U_i=\dfrac{2}{\left(2\alpha t_f\varepsilon_{Si}+\dfrac{\varepsilon_{Si}}{C_{oxi}}\right)t_s}$

$$\psi_s''(y)-A^2\psi_s(y)=A^2B \tag{6.8}$$

where

$$A_i=\sqrt{-\frac{2}{t_s^2}+\frac{2}{\left(2\alpha t_f\varepsilon_{Si}+\dfrac{\varepsilon_{Si}}{C_{oxi}}\right)t_s}}$$

$$B_i=\frac{\dfrac{2(V_{gs}-V_{FB})}{\left(2\alpha t_f\varepsilon_{Si}+\dfrac{\varepsilon_{Si}}{C_{oxi}}\right)t_s}-\dfrac{qN_i}{\epsilon_s}}{-\dfrac{2}{t_s^2}+\dfrac{2}{\left(2\alpha t_f\varepsilon_{Si}+\dfrac{\varepsilon_{Si}}{C_{oxi}}\right)t_s}}$$

For Regions i=1, 2, 3, and 4, the total gate oxide capacitances [9] (considering the fringing effect in region 1 and region 4) in the gate stack are given as follows:

$$C_{ox1} = \frac{2}{\pi} C_{HfO_2}$$
$$C_{ox2} = C_{HfO_2}$$
$$C_{ox3} = C_{SiO_2}$$
$$C_{ox4} = \frac{2}{\pi} C_{SiO_2}$$

where is C_{HfO_2} is HfO_2 capacitance and C_{SiO_2} is SiO_2 capacitance.

The solution to $\psi_s''(y) - A^2\psi_s(y) = A^2B$ can be given as follows [9]:

$$\psi_{si}(y) = m_i \exp(A_i y) + n_i \exp(-A_i y) - B_i \quad (6.9)$$

Region 1: $\psi_{s1}(y) = m_1 \exp(A_1 y) + n_1 \exp(-A_1 y) - B_1$

Region 2: $\psi_{s2}(y) = m_2 \exp(A_2 y) + n_2 \exp(-A_2 y) - B_2$

Region 3: $\psi_{s3}(y) = m_3 \exp(A_3 y) + n_3 \exp(-A_3 y) - B_3$

Region 4: $\psi_{s4}(y) = m_4 \exp(A_4 y) + n_4 \exp(-A_4 y) - B_4$

Continuity equations:

$$\psi_{s(i-1)}(y_i) = \psi_{si}(y_i)$$
$$\psi'_{s(i-1)}(y_i) = \psi'_{si}(y_i)$$

Using continuity equations in the four regions, we get eight equations with eight unknowns:

$$m_1 \exp(A_1 y_0) + n_1 \exp(-A_1 y_0) - B_1 = -\frac{KT}{q} \ln\left(\frac{N_1}{n_i}\right)$$

$$m_1 \exp(A_1 y_1) + n_1 \exp(-A_1 y_1) - m_2 \exp(A_2 y_1) - n_2 \exp(-A_2 y_1) = B_1 - B_2$$

$$A_1 m_1 \exp(A_1 y_1) - A_1 n_1 \exp(-A_1 y_1) - A_2 m_2 \exp(A_2 y_1) + A_2 n_2 \exp(-A_2 y_1) = 0$$

$$m_2 \exp(A_2 y_2) + n_2 \exp(-A_2 y_2) - m_3 \exp(A_3 y_2) - n_3 \exp(-A_3 y_2) = B_2 - B_3$$

$$A_2 m_2 \exp(A_2 y_2) - A_2 n_2 \exp(-A_2 y_2) - A_3 m_3 \exp(A_3 y_2) + A_3 n_3 \exp(-A_3 y_2) = 0$$

$$m_3 \exp(A_3 y_3) + n_3 \exp(-A_3 y_3) - m_4 \exp(A_4 y_3) - n_4 \exp(-A_4 y_3) = B_3 - B_4$$

$$A_3 m_3 \exp(A_3 y_3) - A_3 n_3 \exp(-A_3 y_3) - A_4 m_4 \exp(A_4 y_3) + A_4 n_4 \exp(-A_4 y_3) = 0$$

$$m_4 \exp(A_4 y_4) + n_4 \exp(-A_4 y_4) - B_4 = V_{DS} + \frac{KT}{q} \ln\left(\frac{N_4}{n_i}\right)$$

Solving for the eight unknowns and substituting in the surface potential equation for each region gives us the graph in Figure 6.6.

Figure 6.6 shows that the modeled surface potential is following the same nature as the simulated surface potential. Hence, a physics-based model is derived for surface potential for a Ferroelectric Heterogate Tunnel Field Effect Transistor.

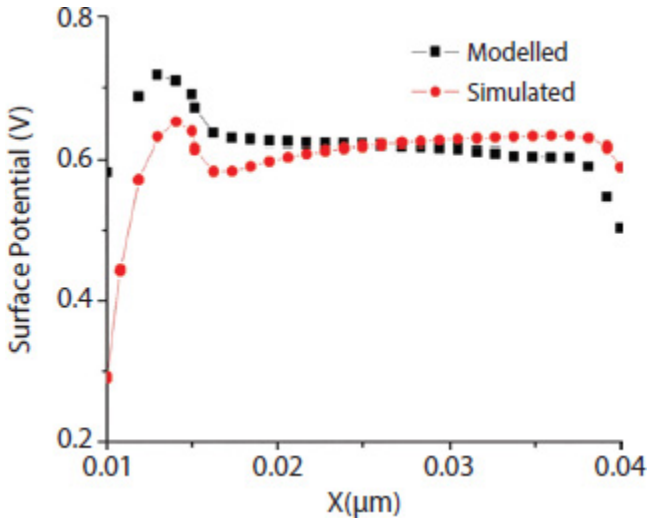

Figure 6.6 Surface potential at V_{gs}=2V.

6.4.2 Study of Electrical Characteristics

6.4.2.1 Average Subthreshold Swing and I_{ON}/I_{OFF}

The final structure gives a better average subthreshold swing of 23mV/ dec and I_{ON}/I_{OFF} value of 3.214×10^{11}, as shown in Figures 6.7 and 6.8. The Ferroelectric Heterogate TFET has the least average SS and second-best I_{ON}/I_{OFF} after conventional ferroelectric TFET. This is due to the increase of I_{OFF}, along with an increase in I_{ON} due to further narrowing of the tunneling barrier in the heterogate structure. This is the best trade-off value pair obtained amongst all the structures that were studied with heterogate structure and ferroelectricity implementation.

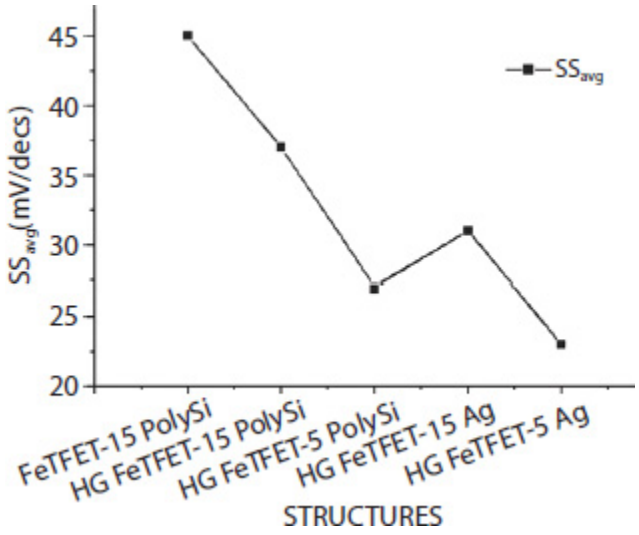

Figure 6.7 Comparison of average subthreshold swing for variants of heterogate ferroelectric TFET and conventional ferroelectric TFET.

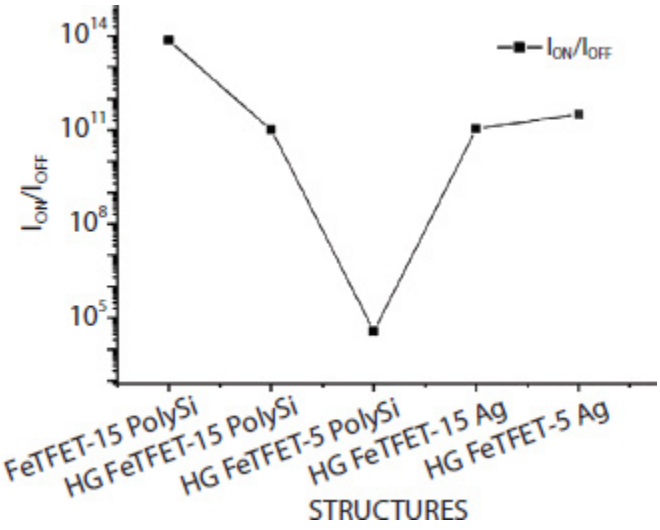

Figure 6.8 Comparison of I_{ON}/I_{OFF} for variants of heterogate ferroelectric TFET and conventional ferroelectric TFET.

6.4.2.2 DIBL

The short channel effect DIBL [9] is studied using TCAD simulations for heterogate TFET and Ferroelectric heterogate TFET by using [11] at varied channel lengths. It is observed that the proposed device is more immune to short channel effects compared with heterogate TFET.

$$\mathrm{DIBL} = -\frac{V_{th}^{DD} - V_{th}^{low}}{V_{DD} - V_{D}^{low}} \tag{6.10}$$

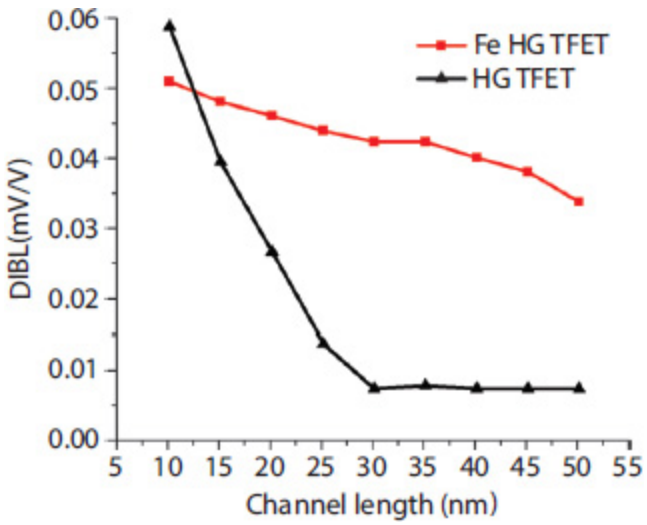

Figure 6.9 Drain induced barrier lowering comparison between heterogate TFET and ferroelectric heterogate TFET for varying channel lengths.

As the channel length is reduced, as shown in Figure 6.9, the DIBL for heterogate TFET is more pronounced below 30nm, but the variation is menial for its ferroelectric counterpart.

6.4.2.3 RDF Effect

The threshold voltage variation due to Random Dopant Fluctuation (RDF) has now become an important concern for modern CMOS technology as the size of the device is scaling up [13]. The fluctuation in the number of dopants and a change in their place, leads to threshold voltage deviation [14]. Band to band tunneling at the source and channel junction depends on the energy bandgaps and electric field that are related to the doping concentration. Hence, TFET is affected by RDF (Random Dopant Fluctuation), which affects transistor properties like threshold voltage, which varies along with the carrier concentration in the channel. Here, the random dopant fluctuation effect is investigated employing Sentaurus TCAD, and it is observed in Figure 6.10 that in Fe HG TFET, threshold voltage is showing more immunity to variation in channel doping when compared to HG TFET. Thus, we obtain a device with high immunity to process variations, i.e., one whose threshold voltage is insensitive to doping variations. The impact of channel length on threshold voltage variation

caused by the RDF is studied. For the sake of our study, we have generated grids 2 nm and 15 nm in size. The simulations were carried out for three different channel lengths for 20 different random dopings and the threshold voltage deviation was determined by using the Constant Current Method (10^{-7}A) to find the threshold voltage. It is observed in Figure 6.11 that the threshold voltage variance is greater for smaller channel lengths. The explanation can be speculated since a small difference can affect a large portion of the channel in short channel devices.

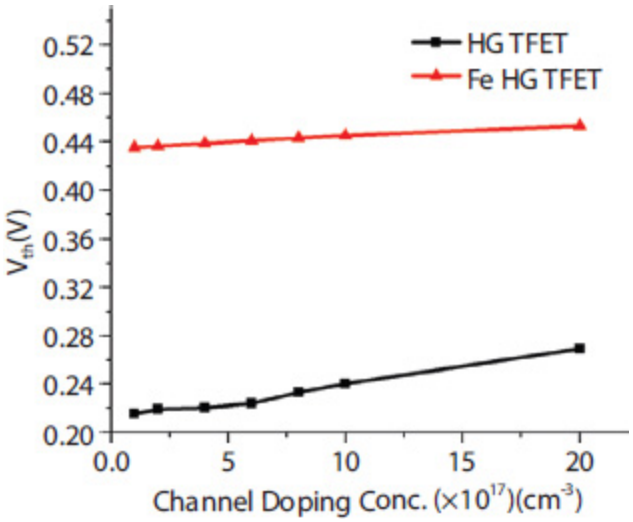

Figure 6.10 V_{th} dependency at varying channel doping concentration for heterogate TFET and ferroelectric heterogate TFET.

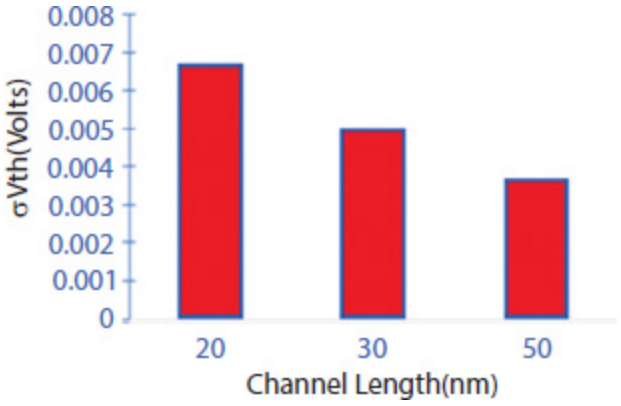

Figure 6.11 Bar diagram of standard deviation of threshold voltage at different channels.

6.4.2.4 Temperature Dependence

In the ON of conduction, an expression of the current rising out of the interband tunneling is given by (6.11) [14]:

$$I_{BTBT} = Q\int G_{BTBT}\, dV \tag{6.11}$$

$$G_{BTBT} = A\frac{|E^2|}{\sqrt{E_G}}\exp\left(-B\frac{E_G^{3/2}}{|E|}\right)$$

As temperature increases, the effective electric field reduces at the source-channel junction, which causes reduction in ON current by reducing the tunneling probability, as shown in (6.12).

$$T \approx \exp\left[-\frac{4}{3}\frac{\sqrt{2m}}{4F\hbar}\left(E_g^{3/2}\right)\right] \tag{6.12}$$

However, this effect is almost but not completely compensated by the decrease in bandgap of the semiconductor with an increase in temperature [11], as shown in (6.13). Hence, at the higher gate voltage, the effect of temperature on ON current is almost insignificant.

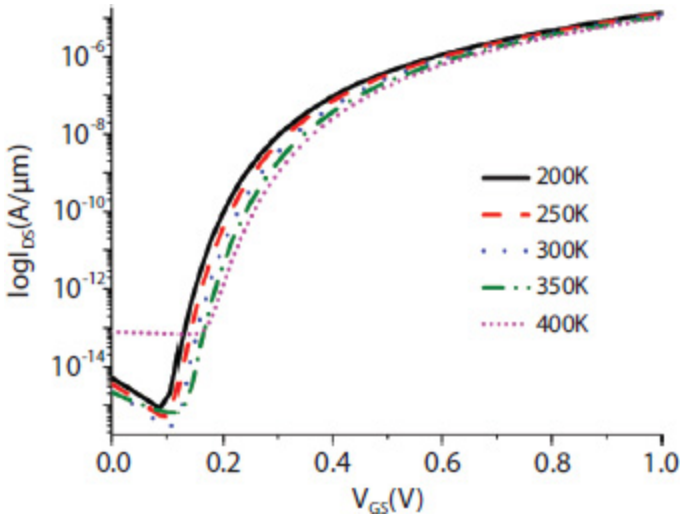

Figure 6.12 Temperature dependence of heterogate ferroelectric TFET.

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta} \tag{6.13}$$

In the OFF state of the device, the diffusion component [15] of the thermal reverse leakage current dominates, which is given by equation (6.14).

The diffusion component is proportional to ni_2 and is dependent on temperature, as shown in (6.14).

While its contribution is negligible for a lower temperature state of the device where BTBT is the prime mechanism, it becomes very pronounced at high temperatures.

$$n_i^2 = N_c N_v \exp\left(-\frac{E_g}{KT}\right) \quad (6.14)$$

Hence, the dependency on temperature at lower gate voltages and almost non-dependency towards temperature is observed in Figure 6.12. It is also seen that ambipolarity is reduced as temperature increases.

6.4.2.5 Study of Interface Traps

At the HfO_2-semiconductor interface and SiO_2-semiconductor interface, the effect of the presence of traps on transfer characteristics is presented in Figures 6.13 and 6.14. The trap concentration is specified per cm^2.

At a smaller concentration of acceptor trap charges, there is a visible decline in BTBT current [16], as shown in Figure 6.13, whereas at a smaller concentration of donor trap charges there is a visible enhancement in BTBT current, as shown in Figure 6.14. This could be explained using the variation in energy bands, as shown in Figure 6.15. The deterioration and enhancement will be more prominent at higher concentrations of the trap charges. The acceptor-type interface traps pull the bands upward and the donor-type interface traps pull the bands downward. As we know, Band-to-Band tunneling current is a function of tunneling width and we see deterioration of ON current as width increases due to acceptor interface trap charges and enhancement of ON current as width decreases due to donor interface trap charges. The reduction in ambipolarity with an increase in concentration of traps is also observed [17].

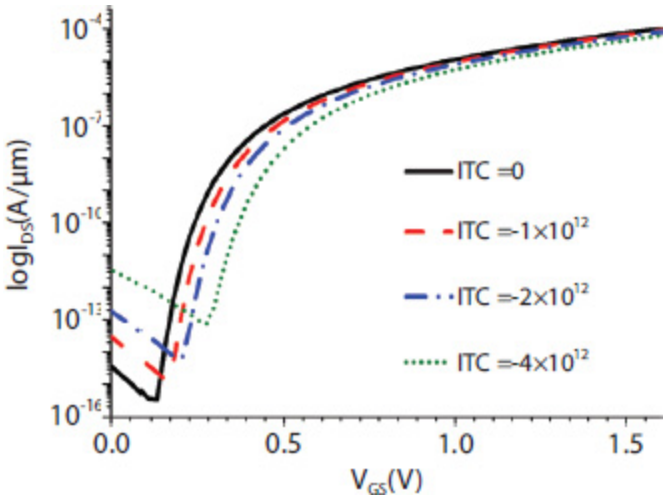

Figure 6.13 Variation of I_d-V_{gs} characteristics due to acceptor interface trap charges.

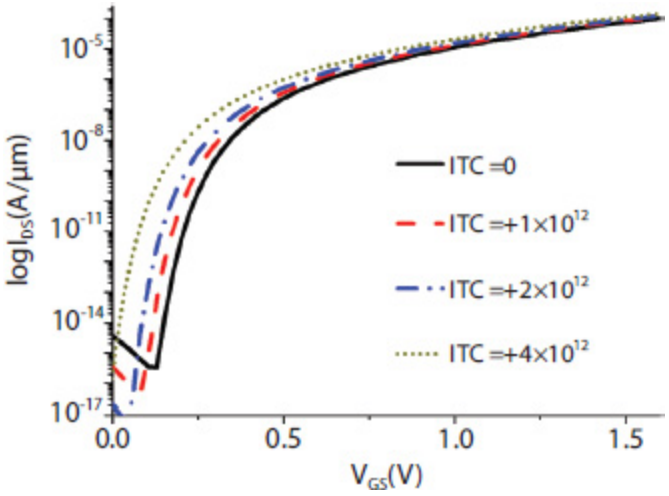

Figure 6.14 Variation of I_d-V_{gs} characteristics due to donor interface trap charges.

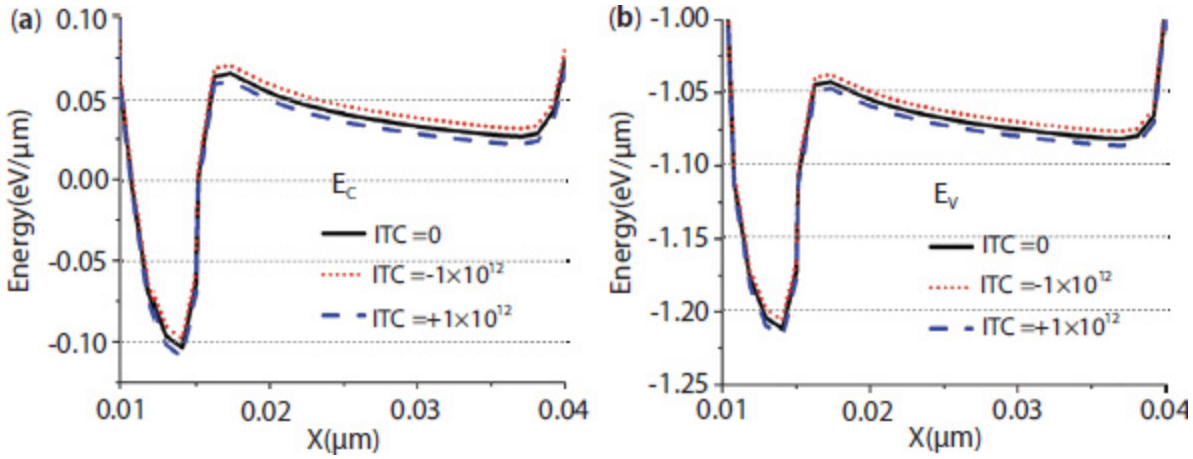

Figure 6.15 (a) Conduction energy band deviation for acceptor (-ve) and donor (+ve) interface trap charges; (b) valence energy band deviation for acceptor (-ve) and donor (+ve) interface trap charges.

The impact of interface trap charges on V_{th} due to variation in band bending [18] is also studied. The bands going higher due to acceptor ($-1x10^{12}$) traps would lead to higher requirements of gate voltage in order to switch the device ON. Similarly, the bands going lower due to donor ($+1x10^{12}$) traps would lead to lower requirements of gate voltage in order to switch the device ON. Hence, as shown in Figure 6.16, the threshold voltage variation is observed in this fashion. It increases with acceptor-type traps and decreases due to donor-type traps.

The influence of traps on the device characteristics also vary along with the temperature [19], as shown below.

In both Figures 6.17 and 6.18, we observe an increase in current and an increase in temperature beyond room temperature in the OFF region or in lower values of V_{GS}. This is because in this region, drain current is originated by SRH recombination which has exponential temperature dependence. However, with an increase in V_{GS}, BTBT dominates and as explained in section 6.4.2.4., ON current is least affected by temperature.

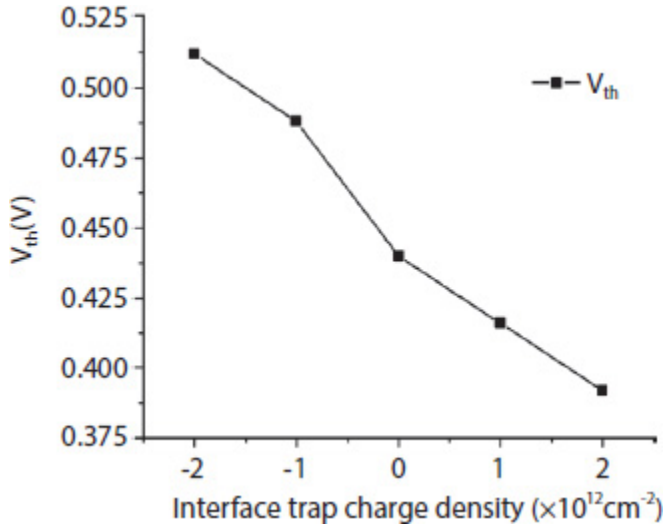

Figure 6.16 Variation of threshold voltage with interface trap charges.

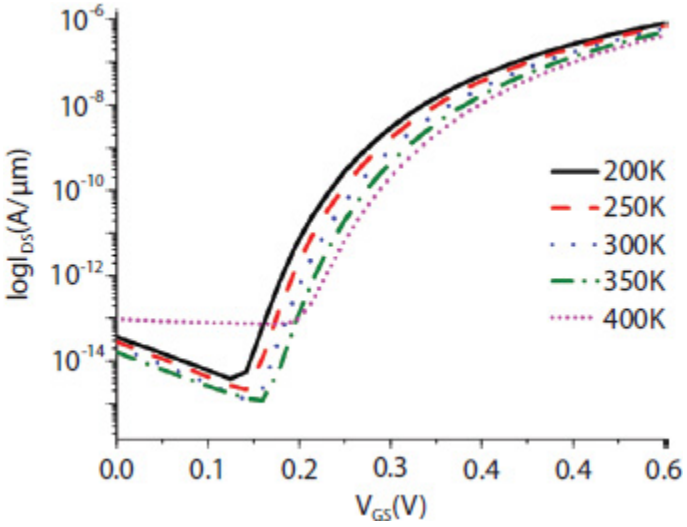

Figure 6.17 I_d-V_g characteristics due to acceptor interface trap charges by variation of temperature.

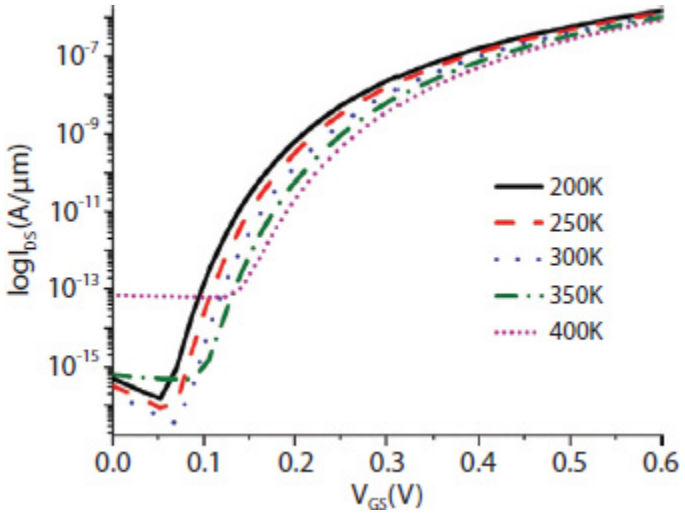

Figure 6.18 I_d-V_g Characteristics due to donor interface trap charges by variation of temperature.

Figure 6.19 shows the variation of drain current effected by interface trap charges as temperature rises. It shows the combined effects of Figures 6.13, 6.14, 6.17, and 6.18. The band bending variation causes the increase and decrease in the current when the interface trap charges are donor and acceptor type, respectively.

The impact of temperature along with interface trap charges on V_{th} is also studied, as shown in Figure 6.20.

The variation of threshold voltage with interface trap charges with temperature in Figure 6.20 can be justified using band diagrams of the device with no traps, acceptor-type traps, and donor-type traps. The rising of the bands with the temperature requires more gate voltage for the overlapping of the source valence band and channel conduction band to overlap for the tunneling current to flow [20], [21]. This is the cause of the increase in threshold voltage of the device.

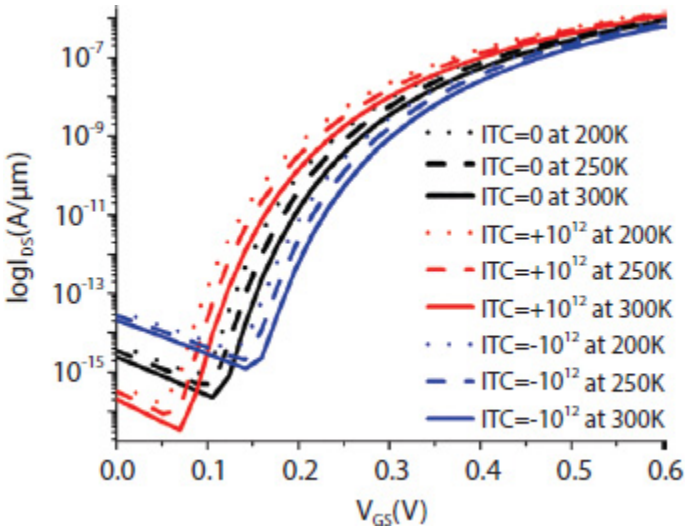

Figure 6.19 I_d-V_{gs} characteristics with temperature variation at different interface trap concentrations.

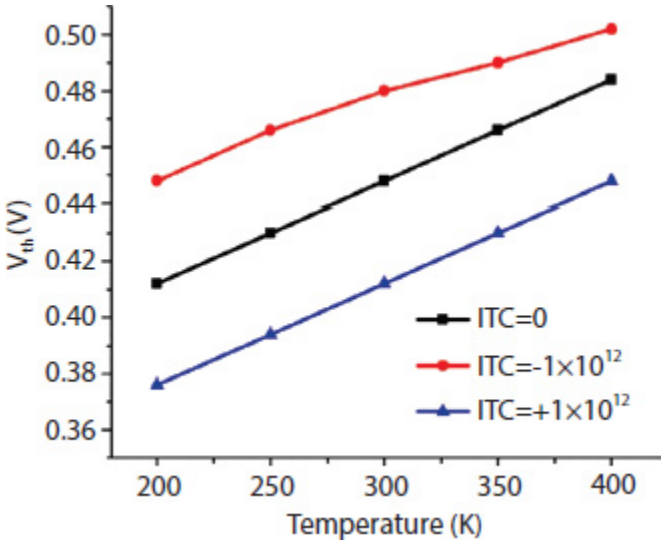

Figure 6.20 Variation of threshold voltage with interface trap charges at varied temperature.

The effect of temperature does not change in acceptor or donor traps, as shown in Figures 6.21, 6.22, and 6.23. In all graphs, as temperature rises, so does the conduction and valence band. It is also observed that the tunneling width decreases as temperature increases. However, this is compensated by the decrease in bandgap as shown in equation (6.13).

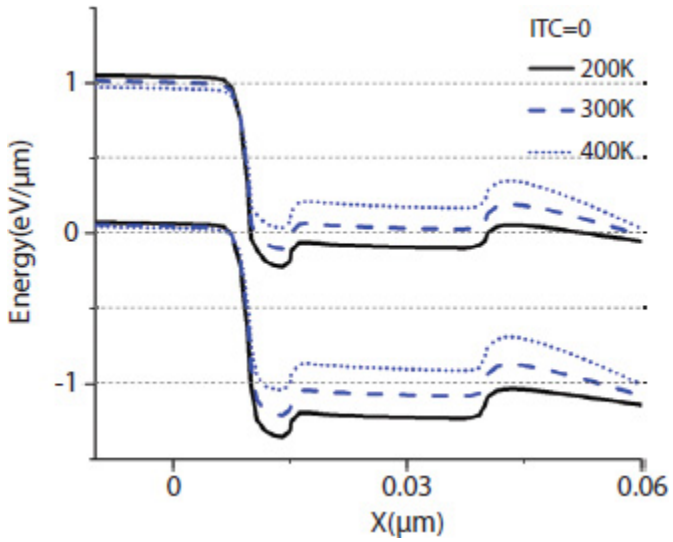

Figure 6.21 Variation of band diagram with temperature for 0 concentration of interface trap charges.

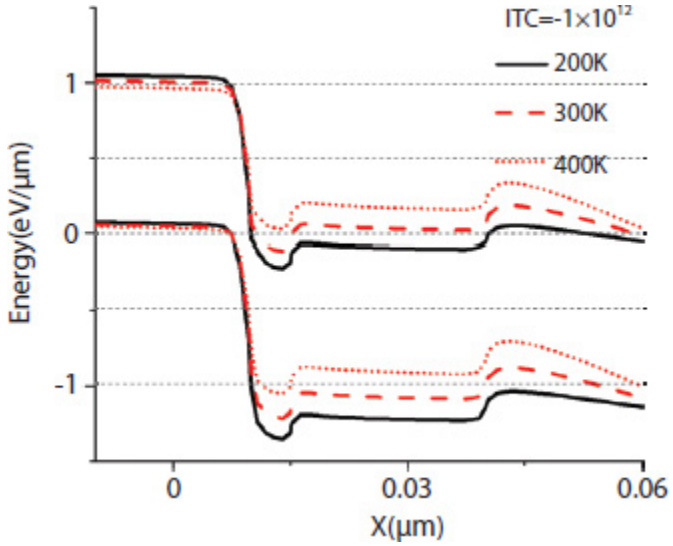

Figure 6.22 Variation of band diagram with temperature for -1x10^{12} interface trap charges.

6.4.3 Memory Window

Figure 6.24 Fe (forward) represents the I_D vs. The V_{GS} graph that is plotted sweeping V_{GS} from -4V to 4V. Fe (reverse) represents the graph plotted by reverse sweeping of V_{GS} from 4V to -4V. The ferroelectric material of the Ferro devices keeps the channel state via the remanent polarization even if the gate voltage is absent. In contrast to a conventional device where the

channel ceases to exist when the gate voltage applied to the device becomes zero, a channel formation takes place in the Ferro devices owing to the up polarization of the ferroelectric insulator [22]. When negative gate voltage is applied, the polarization direction on the ferroelectric material is completely reversed and that is sufficient to induce polarization switching in the ferroelectric layer. This is the reason for hysteresis in the transfer characteristics, subject to the sweep direction of the gate bias. The difference in the graphs in both the directions of sweeping is due to the presence of a memory window in ferroelectric devices. The MW boost mechanism was examined quantitatively based on the detailed FE switching modeling and carrier transport across the additional dielectric layer between the gate metal and the FE layer in integrated FE-FET devices. For that, a new device has been designed, as shown in Figure 6.25, where an extra dielectric (DE) layer (SiO2) is added.

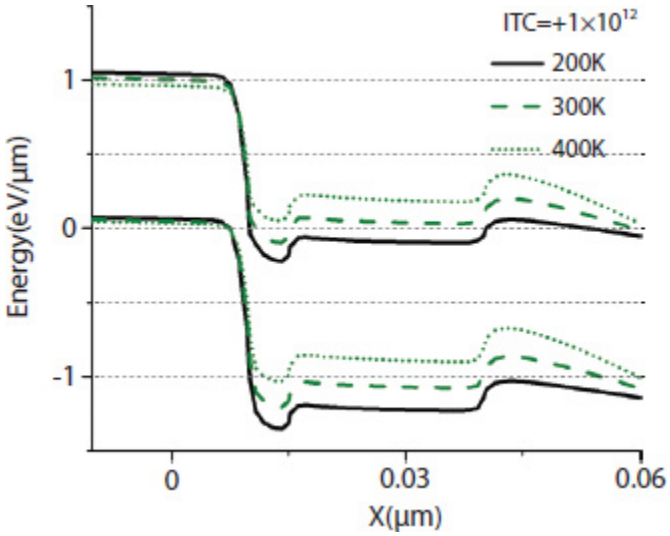

Figure 6.23 Variation of band diagram with temperature for $+1x10^{12}$ interface trap charges.

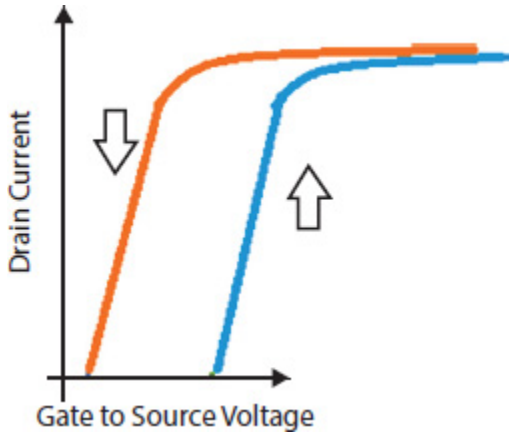

Figure 6.24 Forward and reverse sweep in I_D-V_{GS}.

The Ferro electric layer has positive polarization and negative polarization on the two sides. For switching them, a voltage is required that is more than the coercive voltage (Vcor). In Ferroelectric FET based devices, the fundamental memory window is two times the coercive voltage. The charge injects via the dielectric layer present in between the metal gate and ferro electric layer. Figure 6.26 shows the charge penetration via the thin DE layer of a thickness of 2nm. Under this context, the leakage current through the thin DE layer forms the σ at the DE/FE interface. A portion of the injected charge is retained at the polarization switching, the Vcor rises, and there, MW is also enhanced. The memory window enhances with the thickness of the dielectric layer and that may be attributed to the higher value of σ at the higher DE thickness due to the reduced penetration of the counter-charges (electron) before the gate voltage reaches the –Vcor [23].

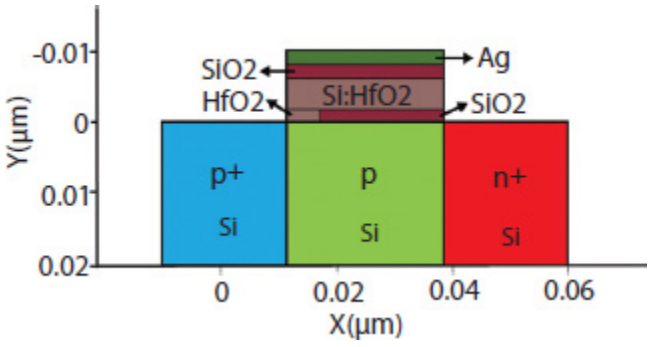

Figure 6.25 Modified structure of heterogate tunnel FET structure with additional SiO2 layer above ferro layer.

The Vcor is given by:

$$Vcor = Vcoro - \frac{\sigma}{Cde}$$

where Vcoro is the coercive voltage in the absence of an extra dielectric layer, σ is the interface charge, and Cde is the capacitance of the SiO_2 based DE layer. This extra voltage drop occurs by the injected charge exchange at the moment of FE switching.

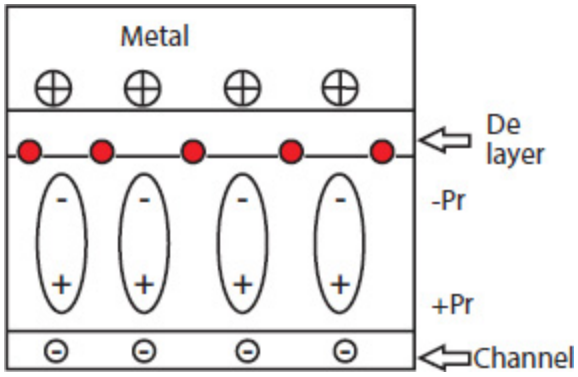

Figure 6.26 Charge penetration through thin dielectric layer (DE).

Table 6.1 Comparative results of memory window.

Devices	Memory Window
HF TFET (Proposed)	1.2 V
HF TFET additional SiO2 layer (Proposed)	2.5 V to 3.2 V

The memory window for a Heterogate Tunnel FET structure and a Heterogate Tunnel FET structure with an additional SiO2 layer above the Ferro layer are compared. The comparison table is given in Table 6.1.

It is observed from Table 6.1 that the memory window for the device with an additional SiO2 layer has been increased and the proposed device with a DE layer is more pronounced for memory applications.

6.5 Conclusion

A comparative investigation of different structures of TFET is carried out employing Sentaurus TCAD simulation tool. It is detected incorporating ferroelectric effect that could give an edge over the other TFET structures in terms of subthreshold swing and I_{ON}/I_{OFF} ratio. This has been proved by the

proposed device that is obtained by implementation of ferroelectric effect on the heterogate structure. It gave the best subthreshold swing value. However, its I_{ON}/I_{OFF} ratio was lower than that of conventional ferroelectric TFET (10^{14}). This is due to higher OFF current in heterogate structures. However, the ratio is still better compared to the rest of the structures. It gave an average subthreshold swing of 23 mV/dec and I_{ON}/I_{OFF} of $3.21x10^{11}$. Studies of short channel effects, random dopant fluctuation effect, temperature dependence, and effect of interface traps have shown that Ferroelectric Heterogate TFET has higher immunity to these factors compared to other conventional devices. The impact of ITC is dominant in the OFF state of the HG ferro TFET, whereas the ON state is almost independent of ITC. This is because the ITC are affecting the flat band voltage in the OFF state and the subthreshold region where the diffusion component is dominant. But, in the ON state, the tunneling component of the drain current is leading. Variation of V_{th} with channel doping is much less, in the range of 0.44V to 0.45 V. A thinner dielectric layer in between the Ferro layer and metal gate is beneficial for an effectual charge booster that causes an increased Vcor, but this may suffer at the peril of charge loss if counter charge inoculation occurs. Hence, careful optimization of the dielectric layer thickness and operation voltage is needed for achieving the best MW.

6.6 Future Scope

This work possesses a wide scope for developing Ferroelectric Tunnel Field Effect Transistors for commercial production. There are future prospects for gate engineered Tunnel FET proposed in this work. Some include the lowering of ambipolar behavior, which is an undesirable factor in various applications. Short retention time is one factor that hinders the practical application of Ferroelectric devices. The retention time is directly proportional to remnant polarization and is inversely proportional to the leakage current and trapping factor. Retention is not up to the mark in the presence of depolarizing fields and off state current. The presence of a depolarized field is due to the finite dielectric constant of the semiconductor. The leakage current is unavoidable at the Metal/Ferroelectric gate and the gate oxide/ Semiconductor interfaces. The

Ferroelectric polarization causes injection of electrons from both the electrode and the semiconductor material and these result in charge trapping phenomena with the ferroelectric gate [24]. So, in order to improve the retention time, the trapping factor and leakage current need to be reduced. Further, fabrication of the mentioned models could lead to better comparison with the simulated and modeled data. The Ferroelectric Heterogate model can be taken to the circuit level to test its performance in real time.

References

1. W. Y. Choi, B. Park, J. D. Lee, and T. K. Liu, “Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV / dec,” vol. 28, no. 8, pp. 743–745, 2007.

2. A. M. Ionescu and H. Riel, “Tunnel field-effect transistors as energy-efficient electronic switches,” *Nature*, vol. 479, no. 7373, pp. 329–337, 2011, doi: 10.1038/nature10679.

3. S. Salahuddin and S. Datta, “Use of negative capacitance to provide voltage amplification for low power nanoscale devices,” *Nano Lett.*, vol. 8, no. 2, pp. 405–410, 2008, doi: 10.1021/nl071804g.

4. K. Boucart and A. M. Ionescu, “Double gate tunnel FET with ultrathin silicon body and high-k gate dielectric,” *ESSDERC 2006 - Proc. 36th Eur. Solid-State Device Res. Conf.*, no. Imm, pp. 383–386, 2006, doi: 10.1109/ ESSDER.2006.307718.

5. W. Y. Choi and W. Lee, “Hetero-gate-dielectric tunneling field-effect transistors,” *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2317–2319, 2010, doi: 10.1109/TED.2010.2052167.

6. P. K. Asthana, B. Ghosh, S. B. Mukund Rahi, and Y. Goswami, “Optimal design for a high performance H-JLTFET using HfO2 as a gate dielectric for ultra low power applications,” *RSC Adv.*, vol. 4, no. 43, pp. 22803–22807, 2014, doi: 10.1039/c4ra00538d.

7. P. K. Asthana, Y. Goswami, S. Basak, S. B. Rahi, and B. Ghosh, “Improved performance of a junctionless tunnel field effect transistor

with a Si and SiGe heterostructure for ultra low power applications," *RSC Adv.*, vol. 5, no. 60, pp. 48779–48785, 2015, doi: 10.1039/c5ra03301b.

8. A. Saeidi, A. Biswas, and A. M. Ionescu, "Modeling and simulation of low power ferroelectric non-volatile memory tunnel field effect transistors using silicon-doped hafnium oxide as gate dielectric," *Solid. State. Electron.*, vol. 124, pp. 16–23, 2016, doi: 10.1016/j.sse.2016.07.025.

9. S. K. Mitra and B. Bhowmick, "A compact interband tunneling current model for Gate-on-Source/Channel SOI-TFETs," *J. Comput. Electron.*, vol. 17, no. 4, pp. 1557–1566, 2018, doi: 10.1007/s10825-018-1236-3.

10. Sentaurus, "Sentaurus sDevice 2015," *Simulation*, no. June, p. 2015, 2009.

11. K. Florent, "Ferroelectric HfO2 for Emerging Ferroelectric Semiconductor Devices," p. 133, 2015.

12. P. Toledano and J. Toledano, *Landau Theory Of Phase Transitions, The: Application To Structural, Incommensurate, Magnetic And Liquid Crystal Systems*, vol. 3. World Scientific Publishing Company, 1987.

13. C. Shin, X. Sun, and T. J. K. Liu, "Study of random-dopant-fluctuation (RDF) effects for the trigate bulk MOSFET," *IEEE Trans. Electron Devices*, vol. 56, no. 7, pp. 1538–1542, 2009, doi: 10.1109/TED.2009.2020321.

14. M. G. Bardon, H. P. Neves, R. Puers, and C. Van Hoof, "Pseudo-twodimensional model for double-gate tunnel FETs considering the junctions depletion regions," *IEEE Trans. Electron Devices*, vol. 57, no. 4, pp. 827–834, 2010, doi: 10.1109/TED.2010.2040661.

15. R. Narang, M. Saxena, R. S. Gupta, and M. Gupta, "Impact of temperature variations on the device and circuit performance of tunnel FET: A simulation study," *IEEE Trans. Nanotechnol.*, vol. 12, no. 6, pp. 951–957, 2013, doi: 10.1109/TNANO.2013.2276401.

16. P. G. Der Agopian *et al.*, “Temperature impact on the tunnel fet off-state current components,” *Solid. State. Electron.*, vol. 78, pp. 141–146, 2012, doi: 10.1016/j.sse.2012.05.053.

17. S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, and S. Datta, “Temperaturedependent I-V characteristics of a vertical In 0.53Ga0.47 tunnel FET,” *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 564–566, 2010, doi: 10.1109/ LED.2010.2045631.

18. Y. Qiu, R. Wang, Q. Huang, and R. Huang, “A comparative study on the impacts of interface traps on tunneling FET and MOSFET,” *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1284–1291, 2014, doi: 10.1109/ TED.2014.2312330.

19. G. B. Beneventi, E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, “Can interface traps suppress TFET ambipolarity?,” *IEEE Electron Device Lett.*, vol. 34, no. 12, pp. 1557–1559, 2013, doi: 10.1109/LED.2013.2284290.

20. J. Madan and R. Chaujar, “Numerical Simulation of N+ Source Pocket PIN-GAA-Tunnel FET: Impact of Interface Trap Charges and Temperature,” *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1482–1488, 2017, doi: 10.1109/ TED.2017.2670603.

21. S. K. Mitra and B. Bhowmick, “Impact of interface traps on performance of Gate-on-Source/Channel SOI TFET,” *Microelectron. Reliab.*, vol. 94, no. November 2018, pp. 1–12, 2019, doi: 10.1016/j.microrel.2019.01.004.

22. J. Y. Kim, M. J. Choi, and H. W. Jang, “Ferroelectric field effect transistors: Progress and perspective,” *APL Mater.*, vol. 9, no. 2, pp. 0–18, 2021, doi: 10.1063/5.0035515.

23. K. Toprasertpong, M. Takenaka, and S. Takagi, “Direct Observation of Interface Charge Behaviors in FeFET by Quasi-Static Split C-V and Hall Techniques: Revealing FeFET Operation,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 2019-Decem, pp. 570–573, 2019, doi: 10.1109/ IEDM19573.2019.8993664.

24. R. S. Lous, “Ferroelectric Memory Devices, How to store the information of the future?,” no. July, p. 23 pp, 2011, [Online]. Available: https://www.rug.nl/research/zernike/education/topmasternanoscience/ns190lous.pdf

Note

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7
State of the Art Tunnel FETs for Low Power Memory Applications

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Abstract

High memory capacity with minimum energy overhead is a critical requirement for the emerging datacentric applications of mobile devices in the consumer market. Conventional memory, based on CMOS technology has reached its final roadblock due to limitations in scaling down the feature size. Tunnel Field Effect Transistors (TFET) are one of the most promising alternatives for such ultra-low power applications. TFETs are widely deployed to implement on-chip memory elements such as SRAMs and DRAMs found in portable devices. The 6T, 7T, 8T, and 10T based SRAM cell designs with tunnel FETs have gained research attention in recent years. This chapter gives an overview on the recent trends in volatile memory cell designs using tunnel FETs and the optimization strategies for enhancing performance.

***Keywords*:** TFET, SRAM, SNM, WNM

7.1 Static Random Access Memory

Static Random Access Memory (SRAM) is an inevitable component in high performance VLSI circuits for a variety of applications. The ability to offer high access speed places these memory elements in the topmost position of the processor memory hierarchy (See Figure 7.1) [1]. The process compatibility with CMOS logic circuits made a smooth integration of

SRAM memory cells in conventional VLSI circuit fabrication without incurring any additional processing costs [1].

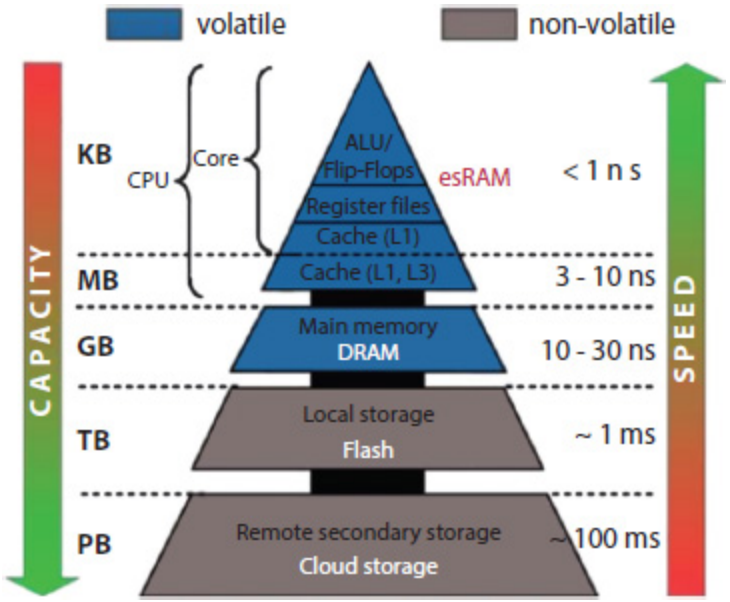


Figure 7.1 Memory hierarchy [4].

SRAMs are the most critical component that occupy more than 90% percent of the chip area and cause very high-power dissipation in processor and System on Chip (SoC) designs [2]. Therefore, SRAM cell optimization is of the utmost importance to realize efficient, high-density, low-power memory circuit designs. To achieve high-density memory, it is essential to maintain the size of SRAM cells as small as possible [3].

To meet the increasing demand for memory capacity, it is essential to have high-density SRAM designs with enhanced performance metrics.

7.1.1 Working of 6T-SRAM Cell

Read/write memory circuits which allow for writing the data and reading the data from the memory array on demand are generally termed as Random Access Memory (RAM). It is a volatile memory which loses its stored data when the power gets turned off. Rather than the sequential access found in older magnetic tapes, it is possible to access any of the cells in the memory array with almost equal access time and that is why it is referred to as RAM. Based on the type of operation of individual memory cells in the array, it can be static RAM or dynamic RAM [5].

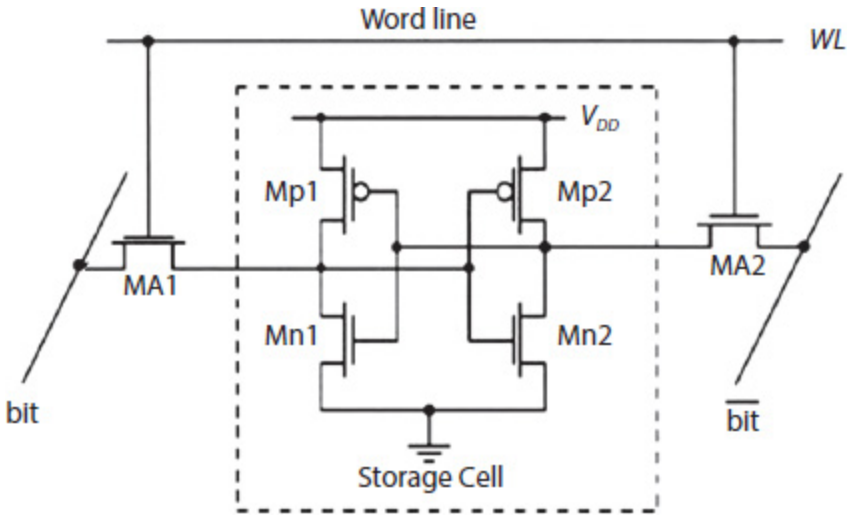


Figure 7.2 Typical structure of a 6T SRAM cell [6].

As the stored data can be held indefinitely, as long as power is provided, without any periodic refreshment, the memory circuit is said to be of the static type. An SRAM cell can execute three different operations, namely, read, write, and hold. The typical structure of a 6T CMOS SRAM circuit is shown in Figure 7.2. It consists of two inverters: cross-coupled and two access transistors. Access transistors are meant for connecting the input or output nodes of the storage cell to the bit lines and are controlled by the word line. By providing a word line input of "1", it is possible to read or write [6].

7.1.1.1 Read Operation

The data present in the memory cell can be transferred to the bit and bit bar line in the read operation. This can be achieved by placing a higher voltage on the word line, thereby turning on the access transistors. Suppose the data stored in the cell is "1", then the voltages in the bit and bit bar line are V_{DD}-V_{th} and 0 V, respectively (Figure 7.3) [6].

7.1.1.2 Write Operation

By placing the word line high and the data to be stored to bit and bit bar lines, in order to write a bit "1" to the memory cell, place a voltage of V_{DD} on the bit line and 0 V on the bit bar line. This will drive the internal node voltages V_1 to high and V_2 to 0 V (Figure 7.4) [6].

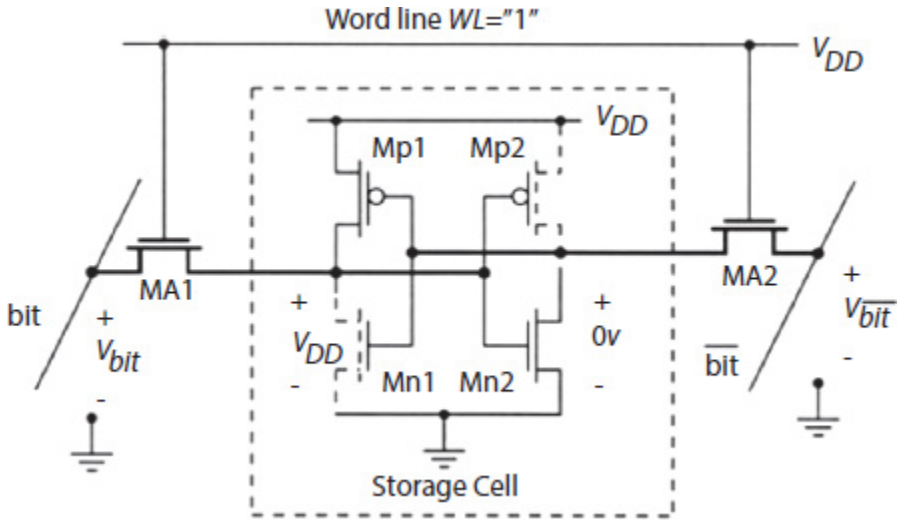


Figure 7.3 SRAM cell under read operation [6].

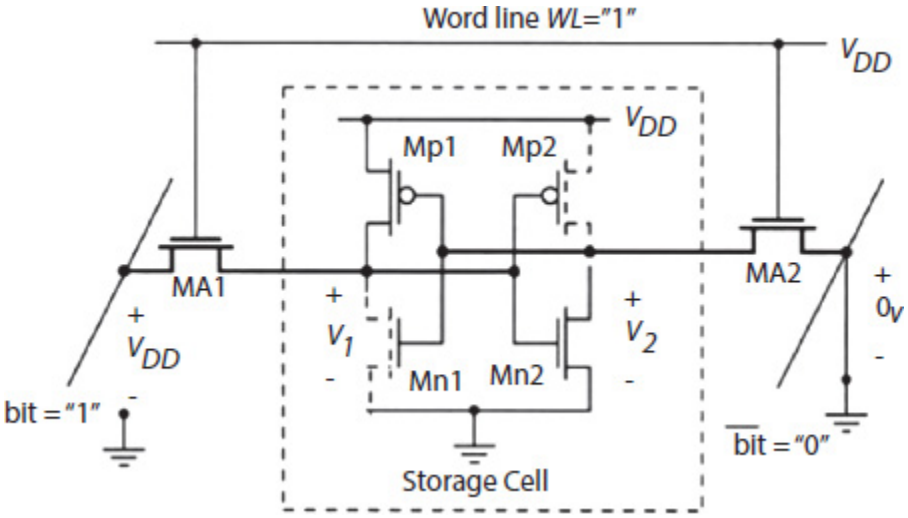


Figure 7.4 SRAM cell under write operation [6].

7.2 Performance Parameters of SRAM Cell

The performance of an SRAM cell is analysed in terms of metrics such as static noise margin (SNM), leakage power, area, etc. Static Noise Margin is termed as the maximum amount of noise voltage that can be managed at both of the input terminals of the inverter so that it maintains a bistable operating point and the storage cell retains the data. In other words, it can be defined as the amount of noise voltage required at the inverter input to flip the data stored in the memory cell. The noise margin of the SRAM cell is generally measured from the "Butterfly curve", a two-wing curve, which

is an intersection of the two curves representing the voltage transfer characteristics of the individual inverters [1]. The graphical interpretation is shown in Figure 7.5.

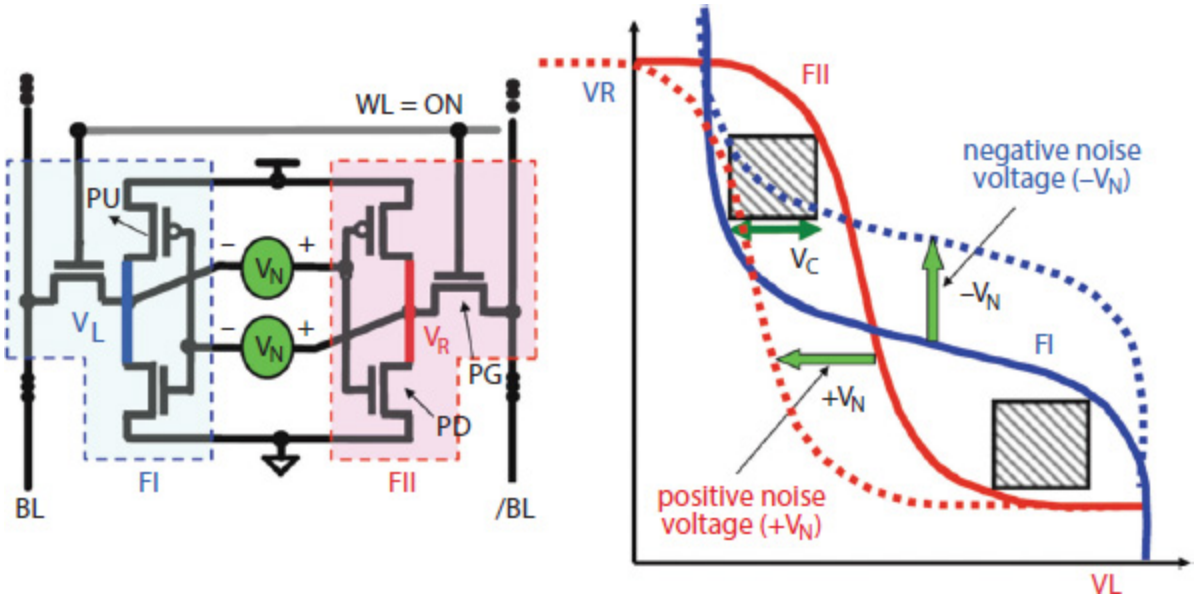


Figure 7.5 Graphical interpretation of SNM [1].

The read noise margin is defined as the side length of the largest square which can be placed within the lobes of the butterfly curve [1] [7]. The read state noise margin is critically dependent on the ratio of the width of pull down to pass transistor, i.e., β ratio, as it determines how much the voltage across the zero storing node will rise during a read operation [1]. The noise margin corresponding to the hold state, i.e., "Hold SNM margin" will be higher than that of the read access time, as there is no rise in potential from the GND level that is happening during this condition [1]. To ensure a proper write margin, it is essential to keep the required ratio of the width of pull up to pass transistor ratio, i.e., γ- ratio, to achieve a robust write operation [1]. Read and write delay is another important parameter while evaluating the performance of an SRAM cell [8].

7.3 TFET-Based SRAM Cell Design

Enabling low voltage operation is one of the key strategies to achieve circuits with low power consumption as it can reduce the dynamic power dissipation quadratically. Thus, the supply voltage for device operation was

reduced considerably to a lower or near threshold range for MOSFET devices. However, reduction in supply voltage results in reduced gate overdrive voltage and reduced ON current of the device [9]. This can be regained up to an extent by reducing the threshold voltage, but this will increase the leakage current drastically. It is reported that lowering the supply voltage to 250 mV from 500 mV with reduced V_{th} increases the leakage power by 275 times in 45 nm commercial bulk-CMOS technology [9]. Devices with steep subthreshold slope are considered to be a suitable candidate to address this issue. It can offer low leakage operation with low threshold voltage and thus power efficient circuits. Among these devices, TFETs are the most promising choice. Being the most critical element in processor designs, SRAM cells must be extremely power efficient. There were several research efforts in the past decade for SRAM cell implementation using TFETs [10] - [19].

Conventional Tunnel FETs suffer from poor drive current, lower I_{ON}/I_{OFF} ratio, lower SS, unidirectional current flow, etc. and hinders the development of efficient memory cells. The forward p-i-n current of TFETs is reported to degrade the stability of the memory cell, leakage power consumption, and static power dissipation [8]. Efficient memory cell design using TFETs is possible only with high drive current, reduced ambipolarity, and proper circuit topology to avoid detrimental effects of unidirectionality [20].

7.3.1 6T SRAM Designs

The TFET based SRAM cell has the same functional units, such as cross-coupled inverters and access transistors to access the memory cell. Figure 7.6 depicts 6T-based SRAM cell design using TFETs [21]. The asymmetry in the doping of source/drain regions of the TFET device causes current flow to be unidirectional with positive drain-to-source biasing [22]. Figure 7.7 depicts the unidirectionality of TFETs.

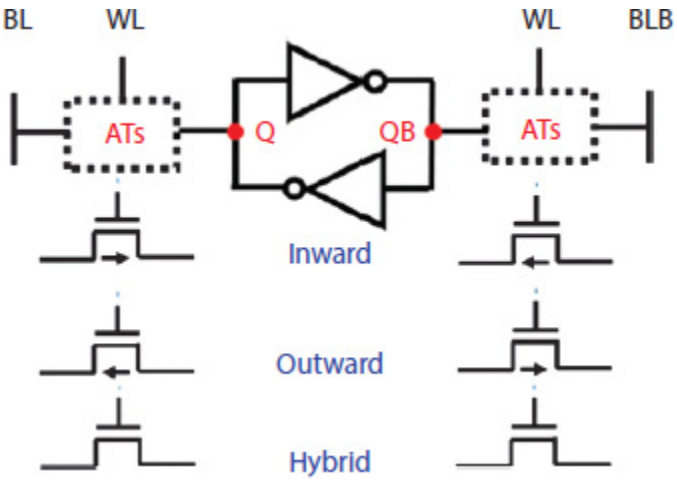


Figure 7.6 6T SRAM with varying access transistor configuration [21].

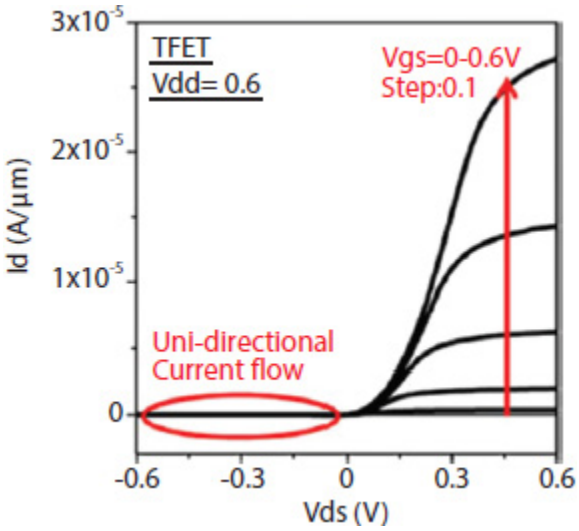


Figure 7.7 Output characteristics of p-n-p-n TFET in double gate architecture illustrating unidirectionality [22].

Unidirectionality of tunnel FETs limits the robustness of memory cells by conflicting read or write requirements in terms of transistor sizing ratios. In TFET based SRAM cell designs, access transistors can be placed either in inward or outward configuration and each of the configurations supports either read or write operations, degrading the other mode of operation. 6T SRAM cells with different configurations of access transistors are reported in the literature. Some of the design as per the literature is shown in Figure 7.6 [21].

The difference in operation of a 6T SRAM circuit based on MOSFET and TFET is analysed in terms of the current flow in the circuit, as shown in

Figure 7.8. In Figure 7.8, (a) and (b) show the CMOS 6T SRAM cell read (stored value is “0”) and write cycles, respectively [9]. In CMOS SRAM, during the read operation, both bit lines are precharged to V_{DD}. Then, both the access transistors are enabled so that the transistor NPDL pulls down the voltage in the BIT line. This can be applied to a sense amplifier to read the data which is stored. To write the data bit “1”, the access transistors are enabled and it will pull the node voltage to a higher voltage, as shown in Figure 7.8b. By increasing the sizing ratios of the transistors used, i.e., β ratio and γ- ratio, the read and write ability of the 6T memory cell can be improved individually at the expense of a large area [9].

Due to the unidirectional current flow in TFET, access transistors can function either in an inward or outward configuration. Figure 7.8 (c) and (d) illustrate the current path in TFET based 6T SRAM cells with an inward configuration of access transistor. Let it be stored with a bit “0”. The read operation in one of the cells is same as that of a CMOS based cell. However, on writing a bit “1”, the transistor AXR is not able to pull down the voltage at node N1 to low, as the transistor conducts current in an inward direction. The transistor AXL must be able to pull the voltage at node N0 higher. To make the internal node voltage high, this circuit relied upon an n-type transistor. Thus, it results in poor write ability for the configuration [9]. To boost the writability, the cell β-ratio should be decreased, which further degrades the read margin. Figure 7.8 (a) and (b) illustrate the 6T SRAM cell design with an outward configuration of access transistors [9].

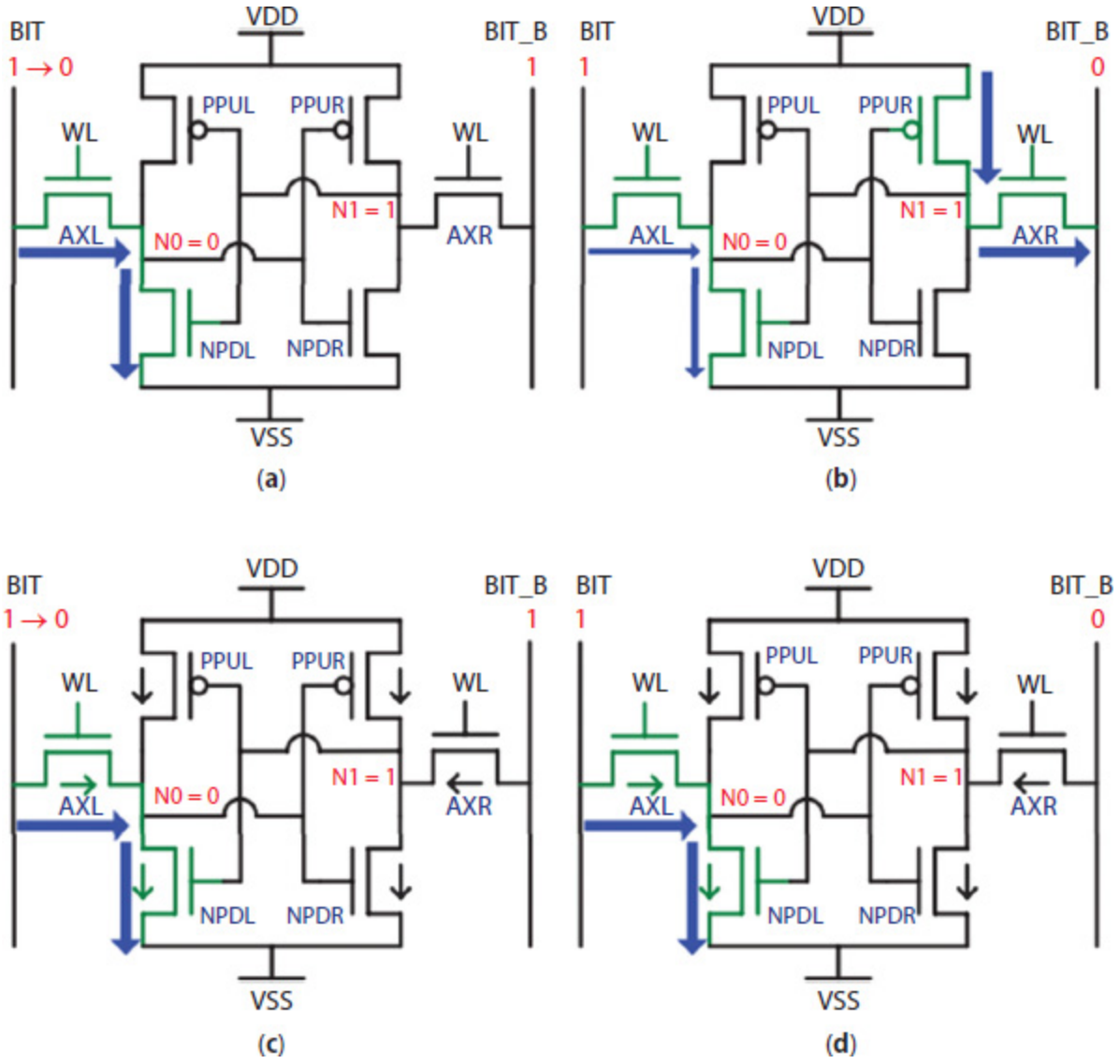


Figure 7.8 Difference in current flow path in 6T CMOS and 6T TFET-based SRAM with inward configuration of access transistor [9].

With an inward access transistor, it is possible to have a robust write operation of bit “1”, as the pass transistor allows it to charge node Q (See Figure 7.9). However, if an outward transistor is used, it will not allow the charging of node Q. No matter which configuration is used, it will result in an efficient single-ended operation. Thus, there are 6T SRAM cell hybrid designs using inverter pairs made of TFETs and access transistors of MOSFETs. Under low-power applications, the current mismatch between MOSFET and TFET technology limits the circuit operation with this hybrid technology [21].

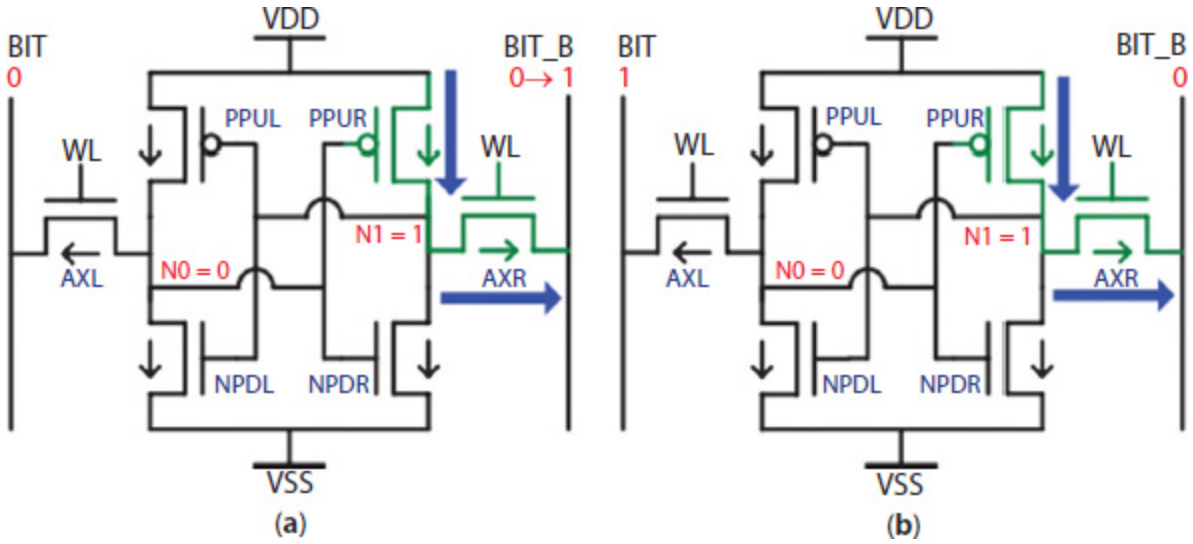


Figure 7.9 6T TFET-based SRAM with outward configuration of access transistor [9].

The limitations of TFET can be resolved up to an extent by the use of device level modifications so that it can be utilized in low power memory cell applications. SRAM cell design with 6T configuration was reported with double gate Si TFETs (See Figure 7.10) [7].

It is difficult to maintain acceptable read and write margins simultaneously with TFET based conventional 6T-SRAM cell designs with both inward and outward access transistor configurations. J. Singh *et al.* in 2010 proposed a novel 6T-TFET based SRAM circuit with improved RNM and WNM. The strategy they adopted was to provide a virtual ground to inverter 1 while writing either the bit '1' or '0' to node Q. It helps to improve the WNM by decoupling of the cross-coupled inverters (Figure 7.11) [7].

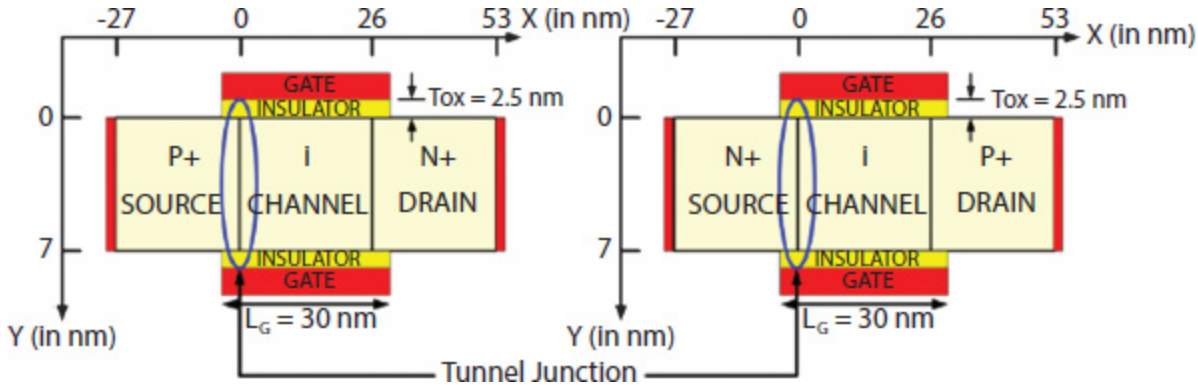


Figure 7.10 Double gate N-type and P-type Si-TFET [7].

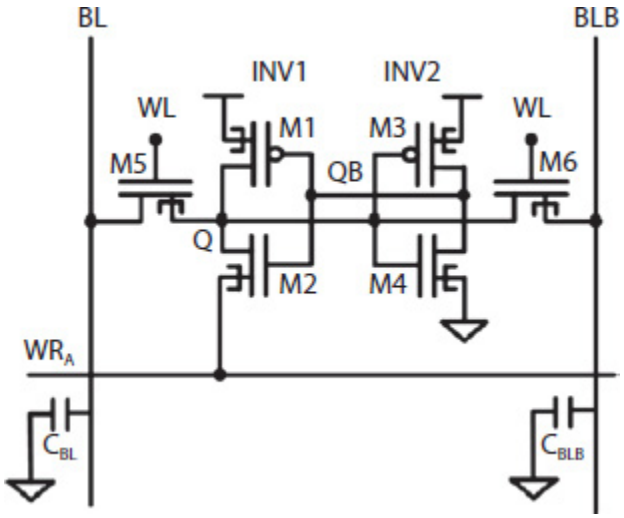


Figure 7.11 Novel 6T-based TFET SRAM cell [7].

The read and write cycle in the proposed design is illustrated in Figure 7.12 [7].

Double gate TFETs were successfully used for the implementation of SRAM cells and it is reported in the literature [3]. They report that even if TFET is a unidirectional device, it does not affect the read stability of the SRAM cell and the inward placement of the access transistor in the design improves the read stability with a degraded write stability [3]. Figures 7.13 and 7.14 represent the working of a double gate TFET based 6T memory cell under read and write modes.

Sebastiano Strangio *et al.* in 2014 reported a 6T SRAM cell using a strained Si channel-based nanowire based TFET structure [23]. They reported that the ambipolarity of the device operation can be mitigated by adopting proper device engineering techniques and unidirectionality can be solved by appropriate circuit designs. Nanowire based device structure can ensure a low leakage operation with smaller subthreshold swing [24]. They implemented 6T SRAM cells with varying access transistor configurations like inward and outward placement [23]. Figures 7.15 and 7.16 depict the circuit configuration and device structure of the nanowire TFET, respectively [23].

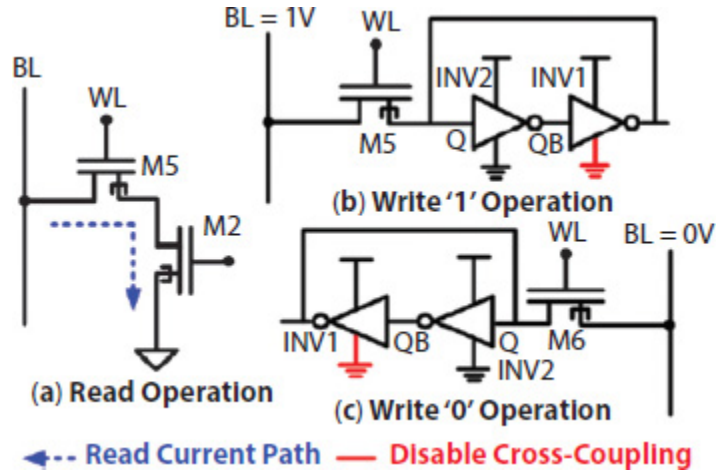


Figure 7.12 Working of modified TFET based 6T SRAM cell during read and write operation [7].

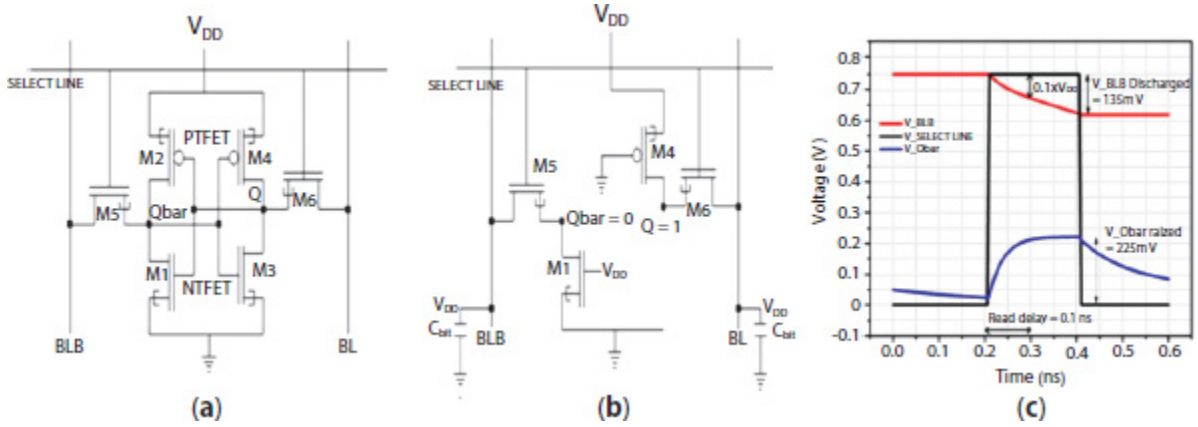


Figure 7.13 (a & b) Read circuit of double gate TFET 6T SRAM cell; c) Voltage levels under read condition [3].

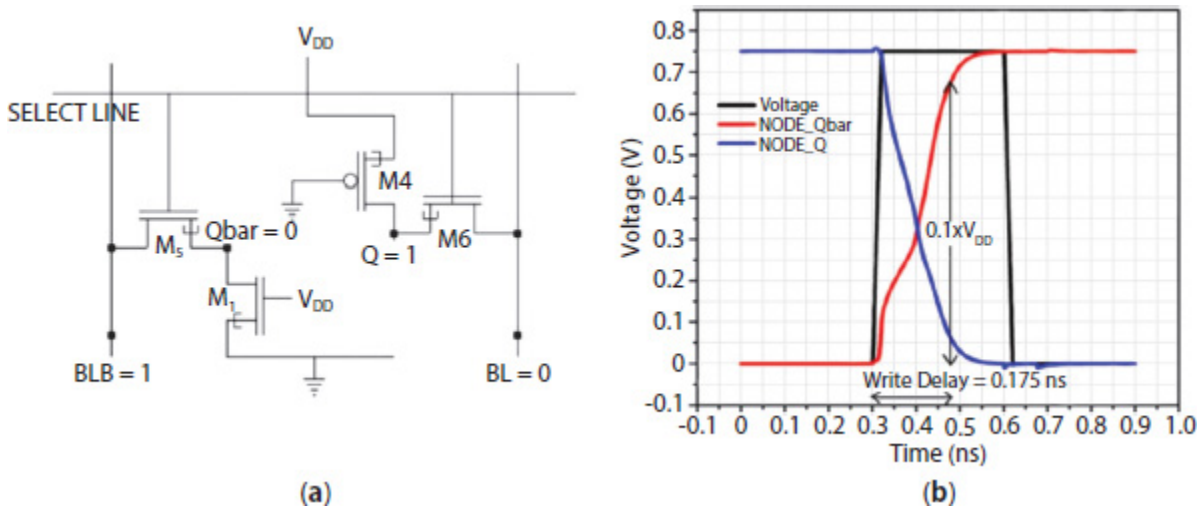


Figure 7.14 (a) Write circuit of DGTFET based 6T SRAM Cell; b) Voltage levels under write condition [3].

G.V Luong *et al.* in 2018 reported the feasibility of a 6T SRAM cell based on strained Si nanowire based TFET (Figure 7.17) [14]. They made use of the outward configuration of n-TFET based access transistors, provided acceptable operation is ensured by precharging the bit line to half of the supply voltage.

Mohammed *et al.* investigated the viability of a 6T SRAM cell design using GaSb/InAs based TFET structure [25]. This hetero junction results in large drive current for the device due to the broken gap-based band alignment. To ensure better device operation in the sub 10nm regime, a vertical gate architecture with a source underlap architecture is adopted for the memory cell design. In the n-TFET structure, the source is underlapped with an n+ InAs layer and this results in a lower leakage current for the device [25]. Figure 7.18 illustrates the vertical TFET structure adopted in the circuit design [25].

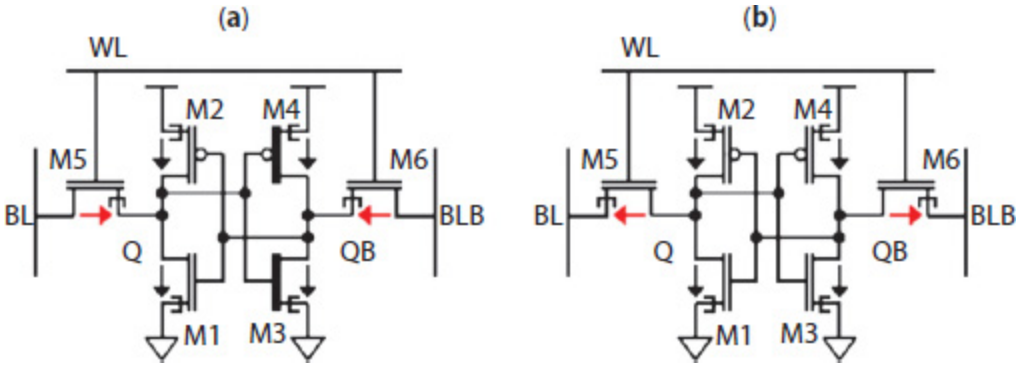


Figure 7.15 6T SRAM Cell with inward and outward configuration of access transistors [23].

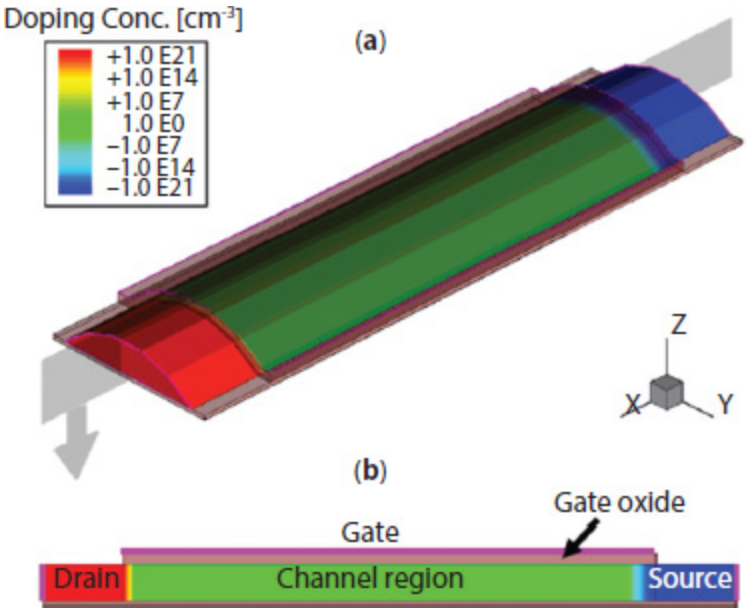


Figure 7.16 Nanowire based TFET for SRAM cell implementation [23].

They have investigated the performance of finFET and TFET based 6T SRAM cells in terms of various metrics such as power dissipation, delay, etc., and they are shown in Table 7.1. FinFETs are able to offer superior performance over conventional MOSFET technology against short channel effects found in scaled devices. However, in the near or sub 10nm regime, FinFET exhibits high off current and TFETs are reported to overcome this limitation [25]. TFET based SRAM cells are reported to have lower area than FinFET based designs. Even though TFETs exhibits lower ON current compared to that of finFET, as the ON/OFF ratio is higher for TFET, it ensures lower standby leakage power and is highly energy efficient. However, as the ON current is lower for TFET, it results in higher delay for

TFET based 6T memory cell design. Tables 7.1 and 7.2 present the reported comparison on SRAM cell design using TFET and fin FET [25].

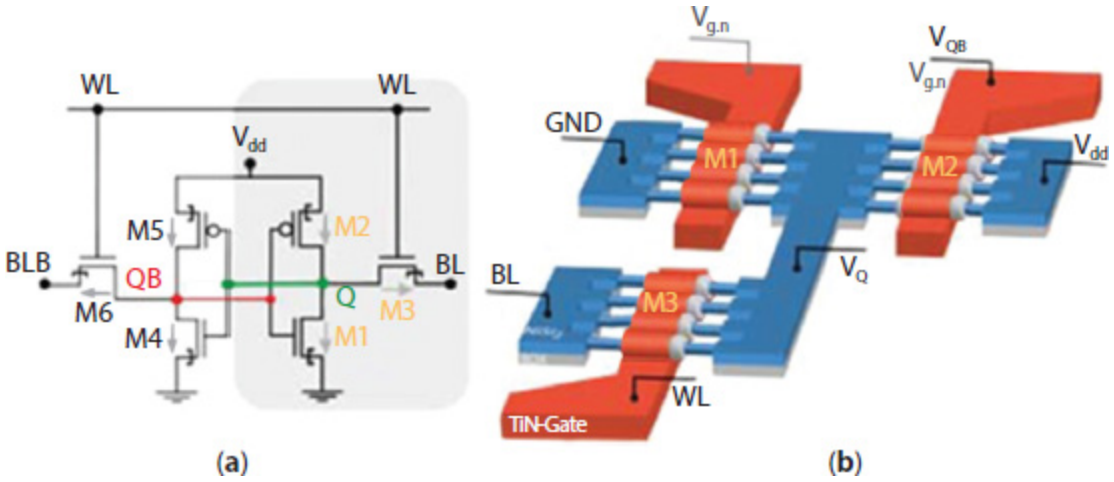


Figure 7.17 (a) 6T SRAM cell implemented; (b) Layout of nanowire TFET [14].

The delayed saturation characteristics and soft transition region causes poor hold or read state noise margins for conventional TFET based designs. The unidirectional characteristics of TFET hinders SRAM circuit design due to the conflicting requirements for read and write operations and area constraints [22].

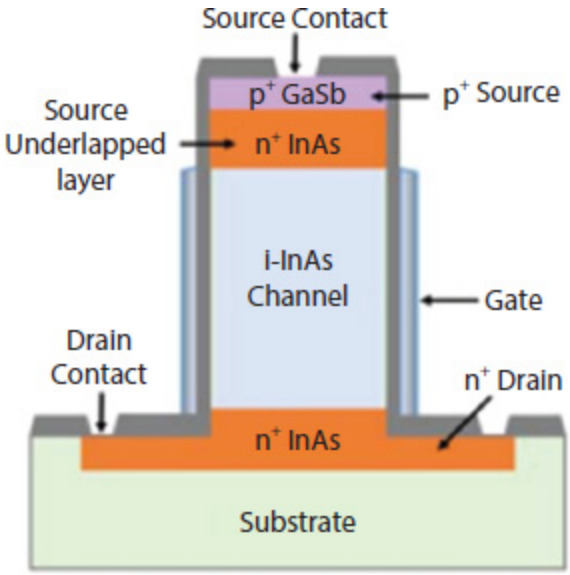


Figure 7.18 GaSb/InAs heterojunction based vertical TFET [25].

Table 7.1 Summary of performance parameters of TFET and FinFET based SRAM [25].

Design	**T-RAM**			**F-RAM**		
Technology	10 nm			10 nm		
Supply Voltage	500 mV			500 mV		
PU:PD:PG	1:1:1	1:5:2	2:5:2	1:1:1	1:5:2	2:5:2
Density	High	Intermediate	Low	High	Intermediate	Low
Dynamic Write Power (nW)	0.562	3.62	4.159	153.048	383.36	522.75
Write Delay(ns)	0.377	0.346	0.43	0.206	0.241	0.309
Dynamic Write Energy (J)	2.11e-19	1.25e-18	1.79e-18	3.15e-17	9.24e-17	1.61e-16
Dynamic Read Power (nW)	1.792	12.728	15.357	94.07	225.50	281.39
Read Delay (ns)	16.56	5.502	5.494	0.928	0.459	0.462
Dynamic Read Energy (J)	2.96e-17	7.02e-17	8.43e-17	8.72e-17	1.034e-16	1.31e-16
Area (μm^2)	0.014	0.026	0.031	0.015	0.033	0.039

Table 7.2 Benchmarking between SRAM cell implementation using TFET and FinFET [25].

Design	**T-RAM**			**F-RAM**		
Technology	10 nm			10 nm		
Supply Voltage	500 mV			500 mV		
PU:PD:PG	1:1:1	1:5:2	2:5:2	1:1:1	1:5:2	2:5:2
Standby Leakage Power (nW)	1.73	3.74	4.55	105.02	243.93	271.65
HSNM (mV)	76.5	101.2	101.4	72.7	96.12	100.8
RSNM (mV)	9.43	48.3	48.5	11.7	28.11	30.38
WSNM (mV)	180.7	82.46	120.24	135.91	200.6	184.33
SVNM(mV)	30.3	93.05	108.96	185.36	194.71	206.16
SINM(mV)	43.58n	3.02 µ	2.97 µ	23.01 µ	116.02 µ	122.5 µ
WTV(mV)	25.12	216.23	213.64	238.52	267.45	256.75
WTI(A)	-55.7n	-3.41 µ	-3.97 µ	-10.1 µ	-17.08 µ	-34.14 µ

7.3.2 7T-SRAM Cell Design

To circumvent the limitations of the 6T-SRAM cell, due to the unidirectionality of TFET, a 7T SRAM cell configuration was reported in the literature. The read delay time is the largest for a 6T SRAM cell with an access transistor in an outward configuration due to the limitation on discharging current [21].

Jheng-Sin Liu *et al.* performed an SRAM cell design using tensile strained Ge/InGaAs tunnel FET and investigated the impact of several types of access schemes on the performance metrics of the SRAM cells. The strain states of Ge were properly chosen to ensure better device characteristics. The design making use of outward access transistors is found to exhibit a higher read-write static noise margin at the expense of increased read delay time [21]. Figure 7.19 shows the TFET structure adopted in the circuit design [21].

The proposed 7T SRAM design consists of an extra transistor with a gate terminal connected to node Q, as shown in Figure 7.20, and the drain terminal is connected to RBL, the read bit line. The source terminal is connected to RWL, the read word line. In a read operation, RWL is at ground potential and RBL is charged to a voltage of V_{DD}. If data is stored at Q, the line RBL will be discharged to the ground. The unidirectional behaviour of TFETs avoids the leakage current in the reverse direction. In addition, the SRAM cell is permitted to stay in the retention mode during the read operation, thus the readability gets improved [21].

The trade-off in read and write requirements of conventional 6T SRAM cells is alleviated by using separate sections for read and write, presented by Yoonmyung Lee *et al.* in 2013. They investigated the feasibility of a novel 7T SRAM cell design using Si/SiGe based hetero junction TFET (Figure 7.21) [9]. The use of hetero structure-based SRAM cell design ensures lower leakage current. The design uses a single decoupled read circuit to ensure better readability [9]. As the read and write operation are enabled by separate current paths, the sizing of transistors can be chosen suitably to support writability. This circuit topology was superior to other 7T SRAM cell implementations that do not use a decoupled read circuit [26–28] or use two transistors for decoupled read operations [29, 30].

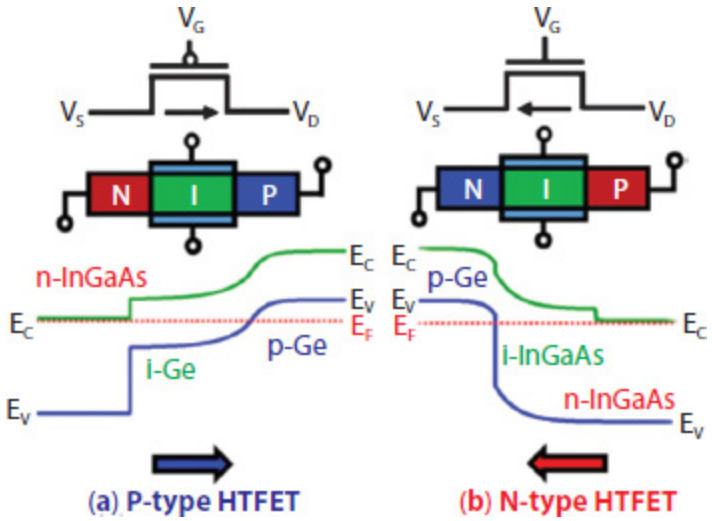


Figure 7.19 (a) p-TFET with InGaAs/Ge heterojunction; (b) n-TFET with InGaAs/Ge heterojunction [21].

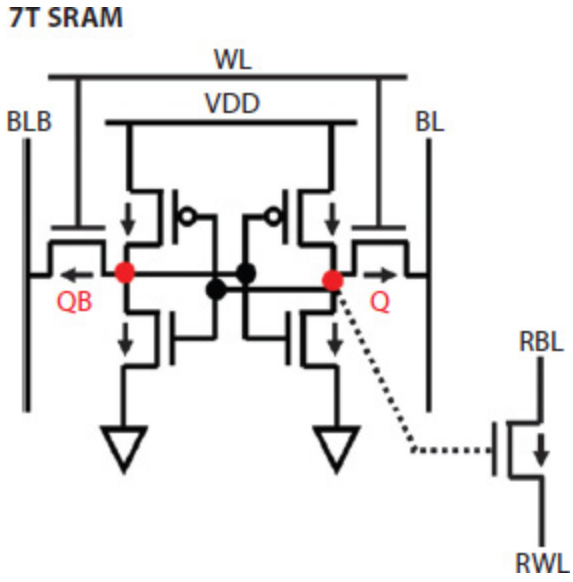


Figure 7.20 7T SRAM cell with read assisted architecture [21].

The degraded write and read operation capability of conventional TFETs can be ascribed to the lower ON current and unidirectionality of the device. These shortcomings are alleviated by the use of a novel dual pocket double gate device structure reported by Sayeed Ahmad *et al.* in 2019. They employed a structure using dual pockets at the source-channel junction, as shown in Figure 7.22. The incorporation of an N+ pocket at the interface results in a higher electric field at the tunnelling junction. This further results in enhanced tunnelling of carriers due to a reduced tunnelling barrier and thereby high drive current for the proposed devices. In the case of a dual pocket structure, the electric field is higher than that of a single pocket based TFET structure [20].

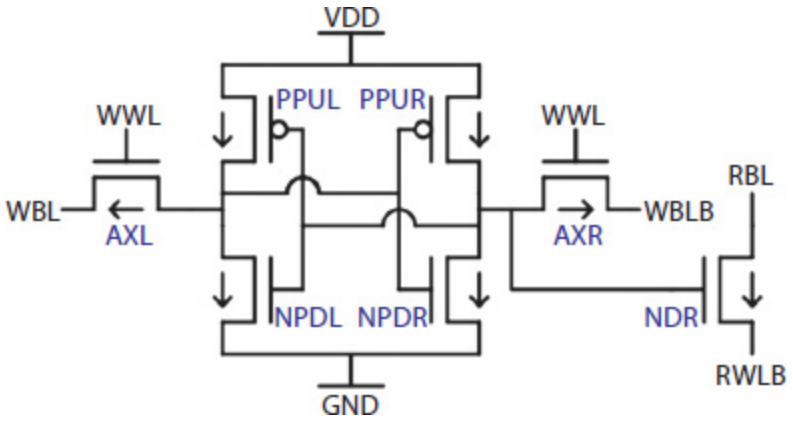


Figure 7.21 7T SRAM cell design [9].

There is substantial increase in ON current for the dual pocket device compared to a single pocket structure, with a negligible rise increase in OFF current of the device. In addition, it showcases better SS, ON/OFF ratio, etc. compared to an SP device. Choosing optimum thickness of the pockets is essential to ensure read and write operations with better stability. With an increase in thickness of Pocket 2, the ON current of TFET increases and the write margin of the device is also improved. However, as the voltage transfer characteristic does not have as sharp a transition as that of a single pocket structure, DPDG TFET based SRAM circuit design exhibits a degraded read static noise margin [2]. The diagram of the conventional and reported 7T SRAM cell is depicted in Figure 7.23 [20].

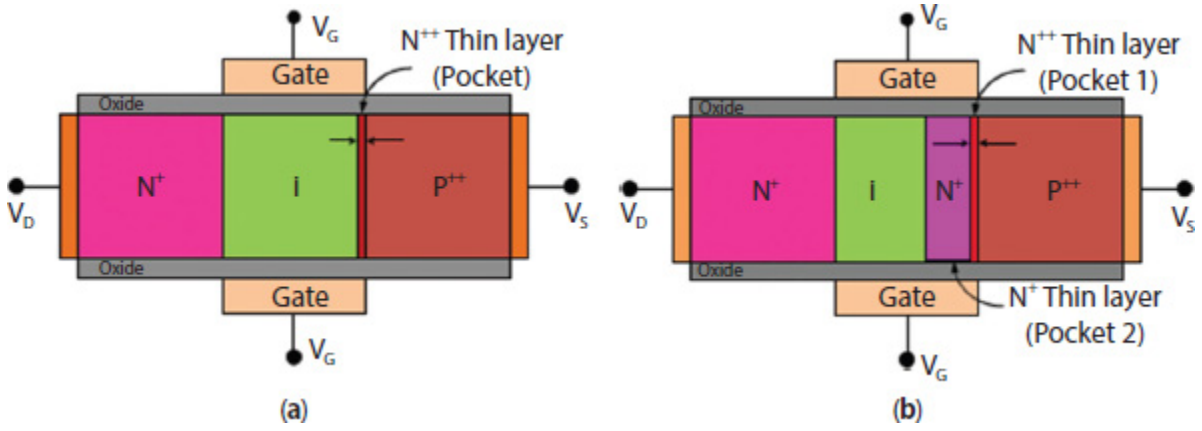


Figure 7.22 (a) SP-DGTFET; (b) DP-DGTFET [20].

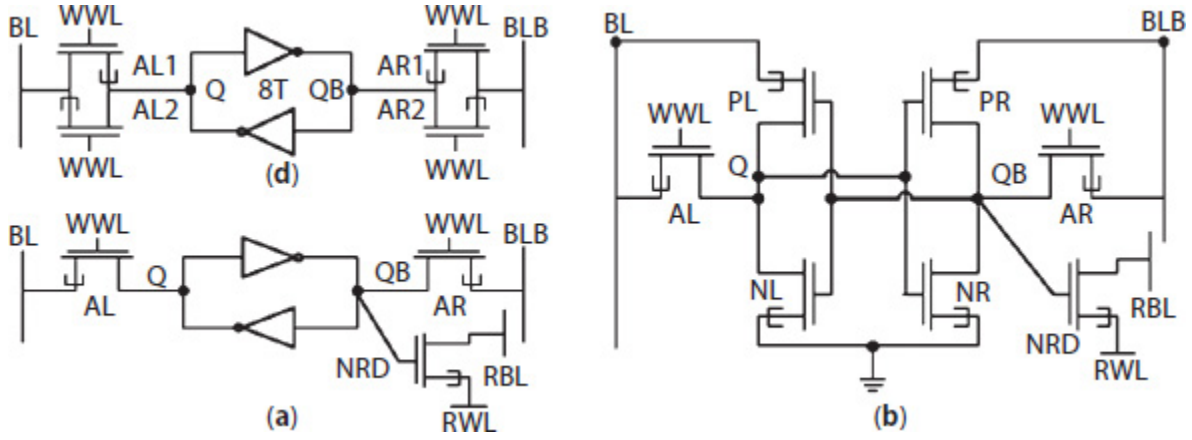


Figure 7.23 7T TFET memory cell designs [20].

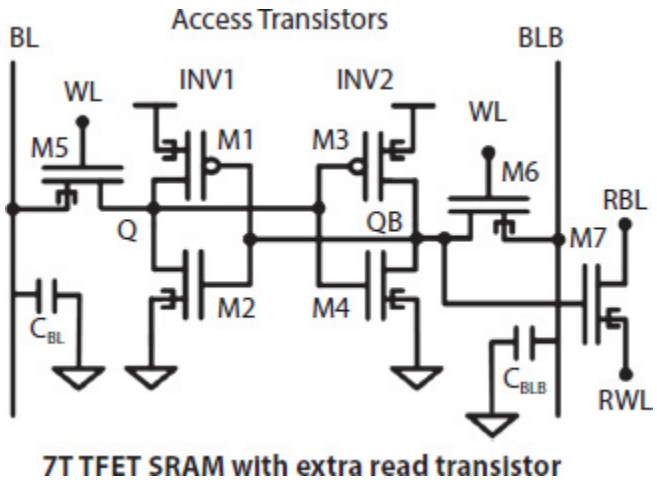


Figure 7.24 7T TFET SRAM with extra read transistor [7].

The unidirectionality of TFETs has some detrimental impacts on the read and write operation of 6T SRAM cells. The degraded stability margins of 6T-SRAM cells are alleviated by a 7T design with an additional read port [7]. Figure 7.24 illustrates a 7T SRAM cell with an extra read transistor.

7.3.3 8T-SRAM Cell

Tunnel FET based 8T and 10T SRAM cells are proposed in the literature [31]. GaSb-InAs heterostructure based double gate TFET (see Figure 7.25) with increased drain current and lower SS are being utilized for realizing SRAM cells. The performance of TFET is reported to be superior to the conventional NMOS in the subthreshold region with high ON current and I_{ON}/I_{OFF} ratio and make it an appropriate choice for low-power applications [31]. However, it is noteworthy to highlight that the saturation voltage, V_{dsat}, of the device has a critical impact on the noise margin of SRAM circuits. As TFETs are low threshold voltage devices, they present a delayed saturation voltage. Moreover, a 6T TFET SRAM with either inward or outward configuration cannot read and write simultaneously.

To overcome the problem of unidirectionality, TFET based 8T transmission gate-based SRAM cells with inward and outward facing access transistors are reported in the literature (refer to Figures 7.25 and 7.26) [22]. The read operation is invoked by activating the inward facing transistors, AXL_{RD} and AXR_{RD}, through the word line, WL. The 8T(10T) SRAM cell has separate ports for both write and read operations [31].

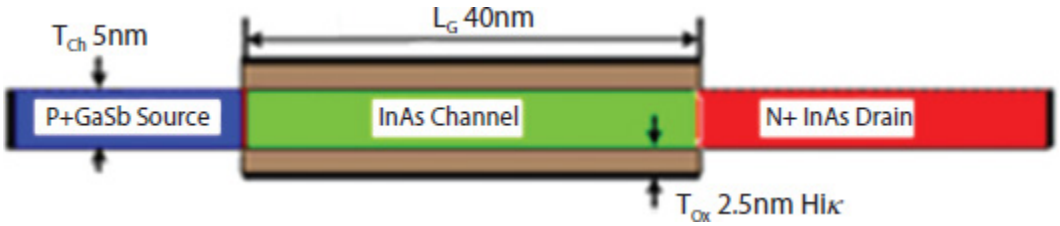


Figure 7.25 Device structure of GaSb/InAs heterojunction based TFET [31].

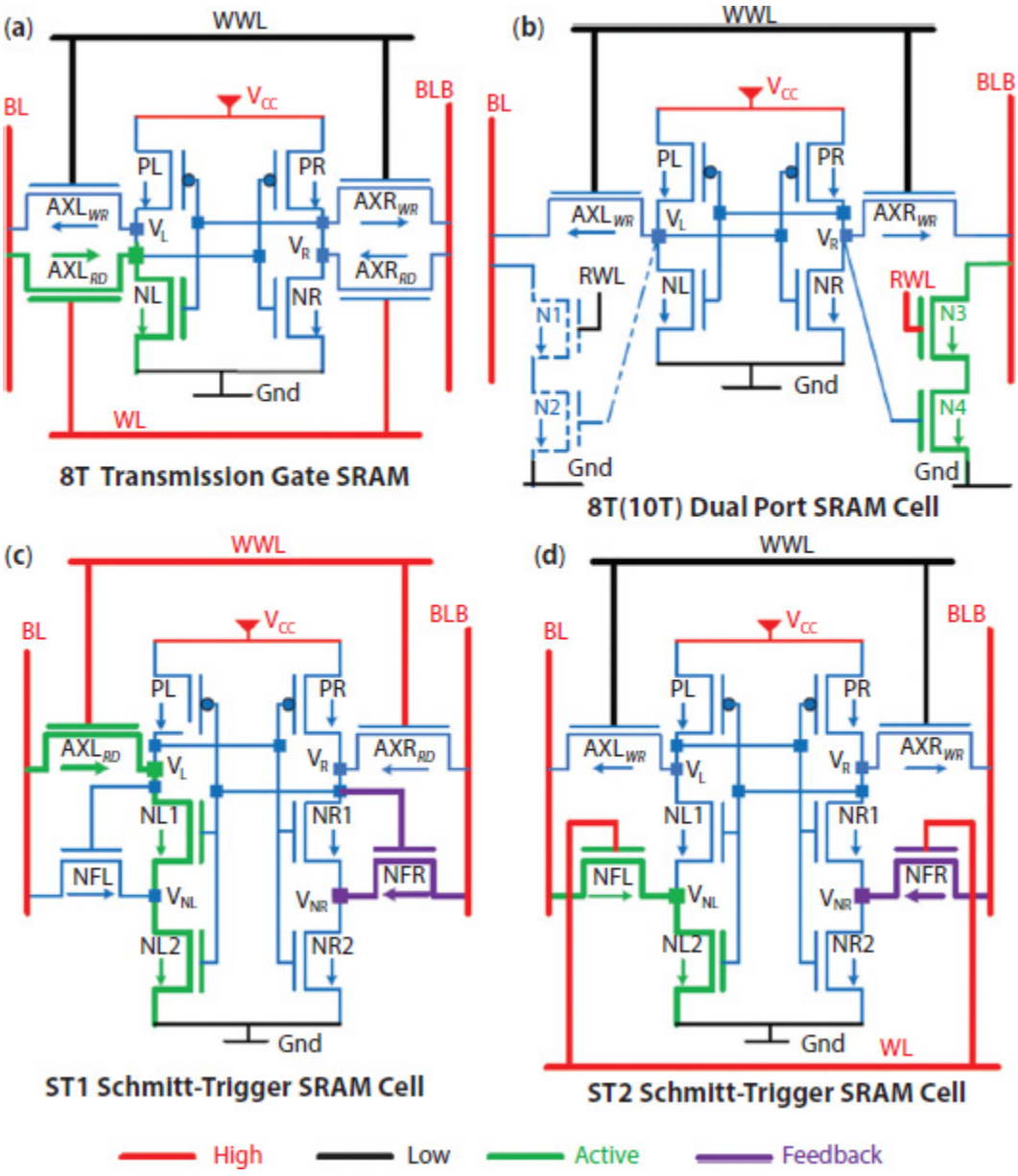


Figure 7.26 8T SRAM cell implementation using TFETs [31].

8T TFET based SRAM cell designs are reported with double gate TFET architectures with pocket doped regions. The various device structures used for conventional SRAM cell designs are illustrated in Figure 7.27. Double gate p-n-p-n TFET is identified as a device with an enhanced current ratio and sub 60 mV. The introduction of n+ pocket raises the lateral electric field, thereby reducing the tunnelling width and enhancing the drain current of the TFET [22].

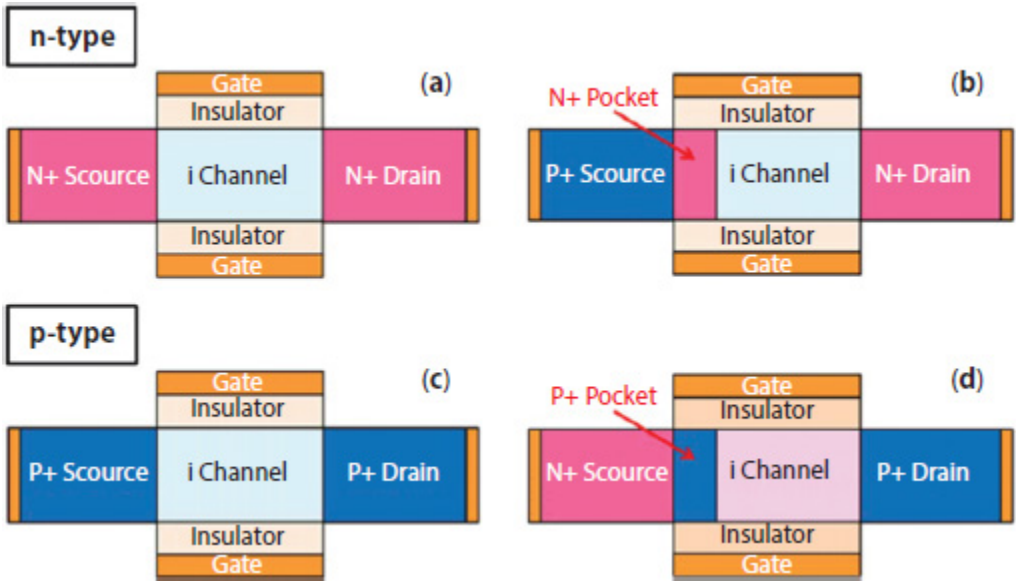


Figure 7.27 (a) n Channel FET; (b) n-type p-n-p-n based TFET structure; (c) p Channel FET; (d) p-type p-n-p-n based TFET structure [22].

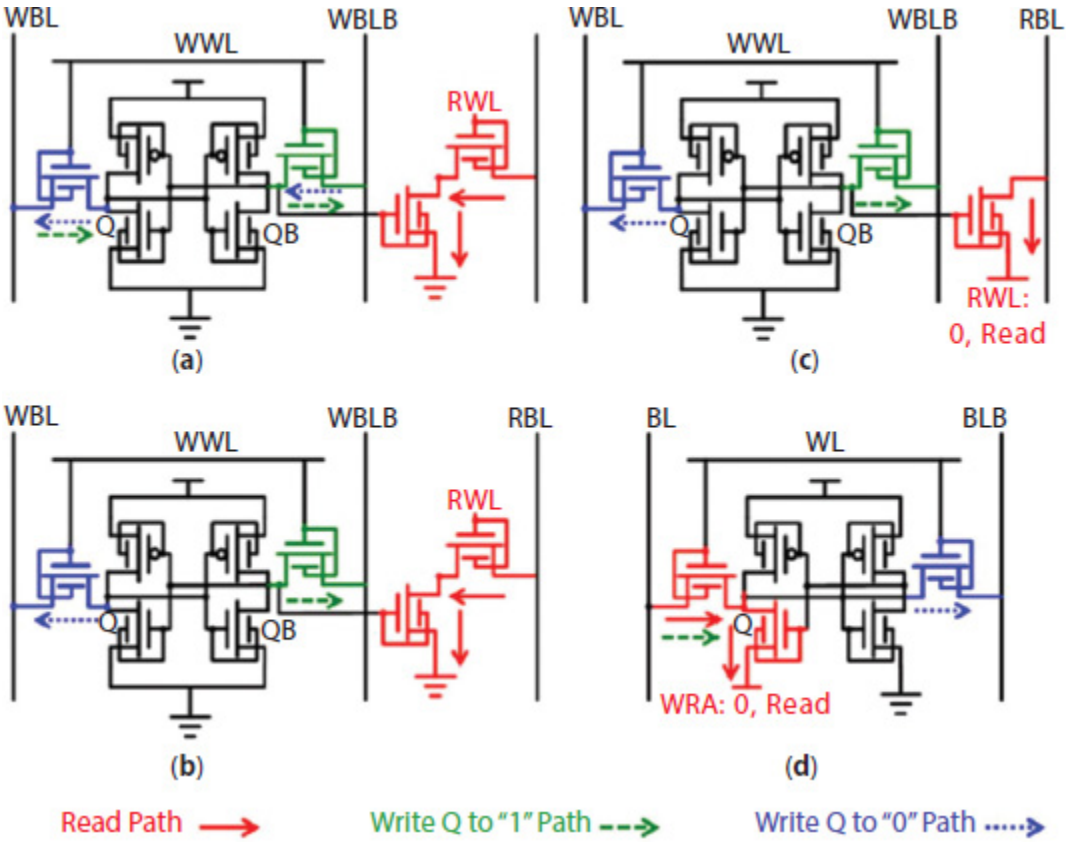


Figure 7.28 (a) MOSFET based 8T SRAM; (b) TFET based 8T SRAM; (c) TFET based 7T SRAM [9]; (d) TFET based 6T SRAM [22].

The 6T TFET SRAM cell makes use of an access transistor in an inward configuration for read. This topology results in large read-disturb and exhibits worse RSNM. In both 7T based and 8T based TFET, the storage node is decoupled from the read current path by means of a read buffer (Figure 7.28). Thus, the read-disturb issue is alleviated here. The 7T TFET SRAM cell makes use of one transistor, whereas an 8T TFETSRAM uses two transistors in a stacked mode to carry out the read operation [22].

The stability issue with the conventional 6T TFET SRAM cell is eliminated by the addition of two FETs to the 6T configuration by Leland Chang *et al.* in 2005 [32]. It enables a read operation that does not interrupt the internal nodes of the cell. This helps to prevent the worst-case stability condition. The structure of the memory cell is shown in Figure 7.29.

Andrei Vladimirescu *et al.* in 2015 reported an 8T SRAM cell design implemented using a 28 nm TFET technology. Figure 7.30 illustrates the

proposed SRAM cell structure [33, 34]. A dual port configuration is adopted for the memory cell design.

Mounica Patnalaa *et al.*, in 2018, reported the implementation of an 8T SRAM cell using GaN TEFTs. The use of III-V material systems for source or drain regions was reported to ensure high drive current for TFETs at a lower supply voltage regime (Tables 7.3 and 7.4). They compared the performance of 8T based SRAM cells with FinFET and graphene-based FETs [35]. The work reports the lowest delay for TFET based 8T SRAM cells. Figure 7.31 illustrates the proposed circuit design.

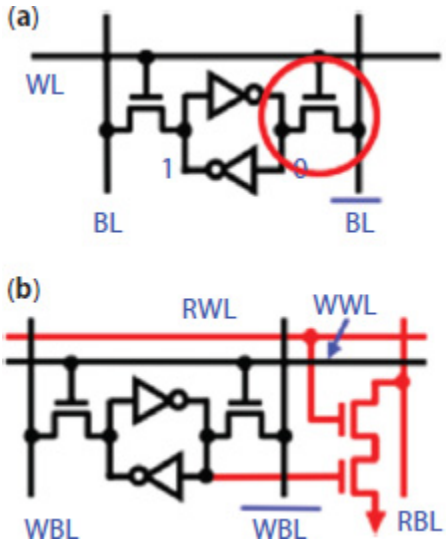


Figure 7.29 (a) 6T SRAM; (b) 8T SRAM cell design [32].

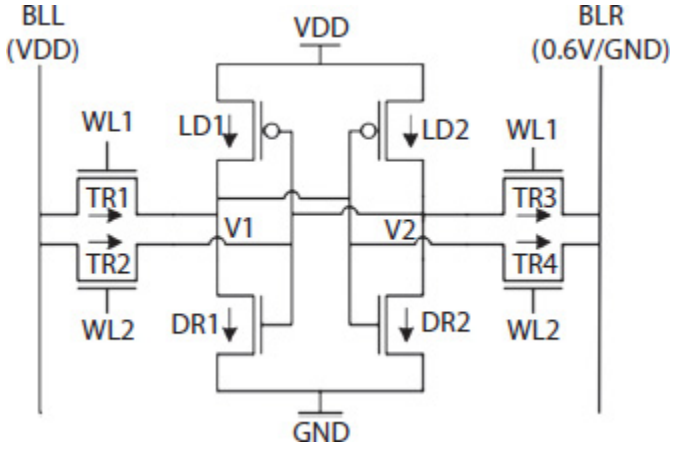


Figure 7.30 8T SRAM cell design [33].

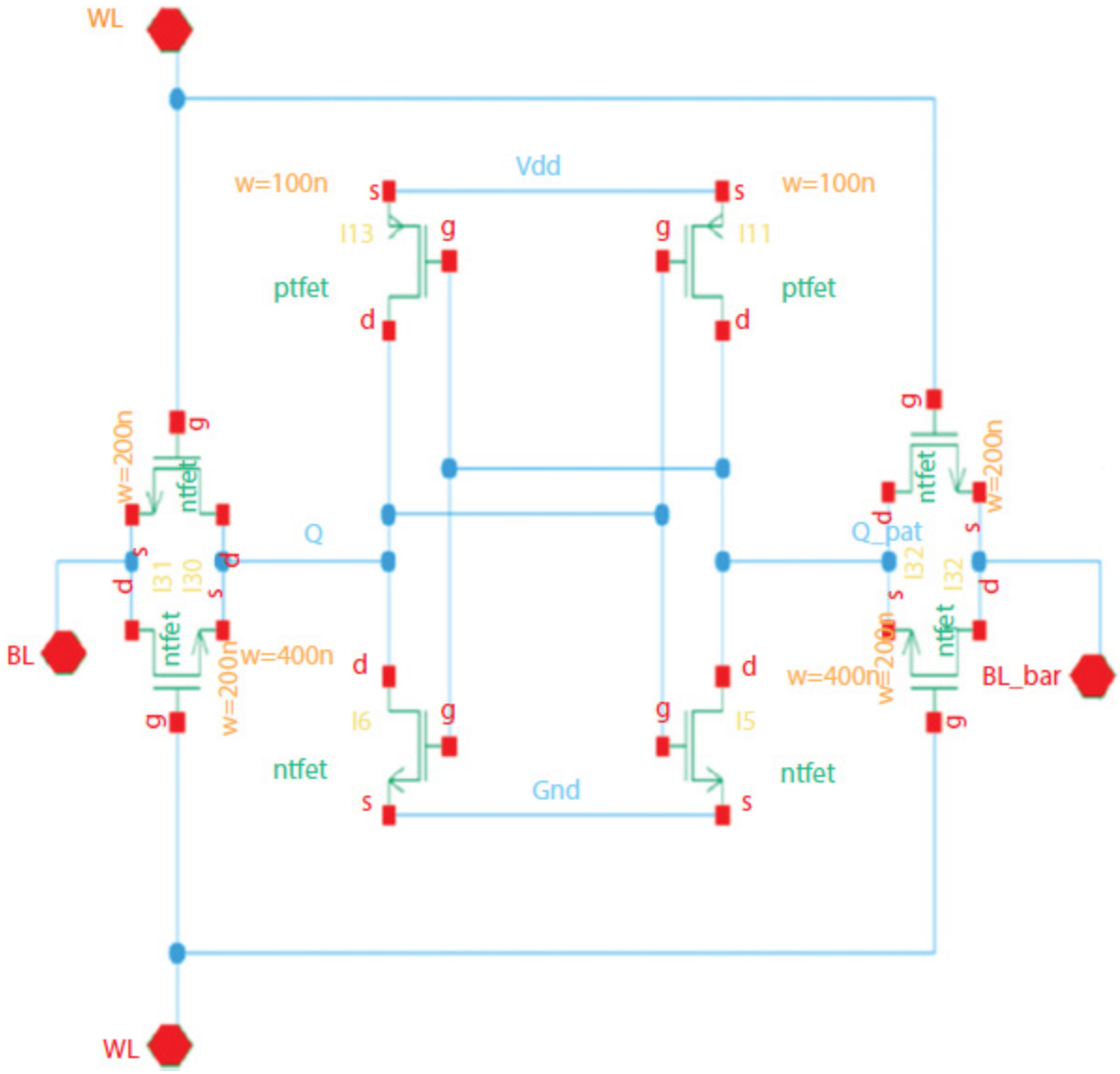


Figure 7.31 8T SRAM cell design using GaN TFET [35].

Table 7.3 Comparison on SRAM circuits based on GaN TFET, FinFET, and graphene transistors [35].

	GaN TFET [36, 37]	**FinFET [38]**	**GNRFET [38]**
Power Consumption (nW)	2.03	34.1	8.23
Power Dissipation (nW)	0.2	10.23	0.401
Delay	1.3	4.65	3.75

Table 7.4 Comparison on SRAM circuits based on GaN TFET, FinFET [35].

	GaN TFET [39]	**FinFET [40, 41]**
Supply Voltage (V)	0.6	0.85
RSNM (mV)	230	261.81
WSNM (mV)	350	273.58
Dynamic Power (nW)	1.07	670
Leakage Power (nW)	2.9	64
Write Delay (ps)	26	29.3
Read Delay (ps)	14.2	25.7
SNM (mV)	200	202

7.3.4 10 T-SRAM Cell

The forward p-i-n current in TFET by virtue of the asymmetry in the source and drain region doping reported to deteriorate the read performance of 6T and 7T SRAM cells and Schmitt trigger-based 10T SRAM cells with inward and outward facing access transistors. To further improve the read stability, a combinational access 10T SRAM cell with an extra read port is reported in the literature [42]. To eliminate the forward p-i-n current, the drain terminal of the access transistor was made higher than that of the source. Still, the poor drive current of the device results in a degraded write ability of the proposed device. Figure 7.32 shows the structure of a combinational access 10T SRAM cell. In the circuit topology, the drain of the upper access transistor has a connection storage node. Meanwhile, the source terminal of the grounding transistor is at ground potential. Drain potential of each n-TFET transistor is always made higher than that of the source potential to prevent forward p-i-n bias [42].

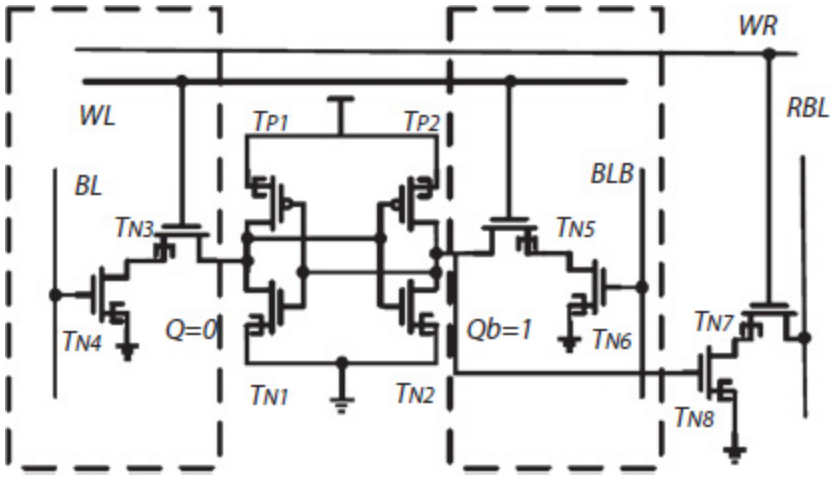
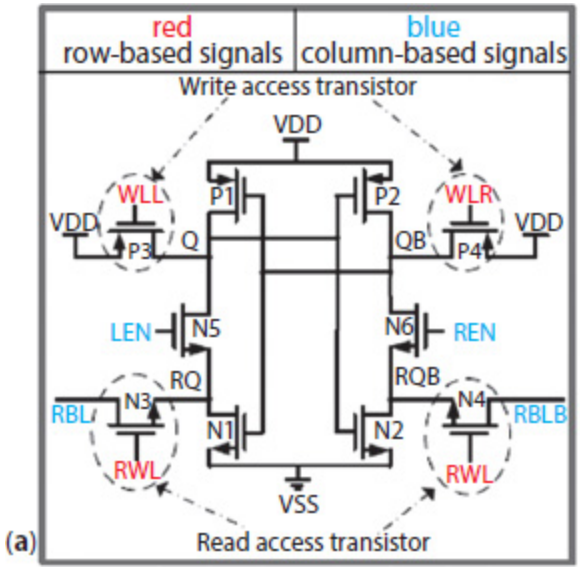


Figure 7.32 Combinational access 10T SRAM cell [42].

Zhiting Lin *et al.*, in 2021, reported SRAM cell design with an InAs-based double gate TFET structure [8]. The proposed cell (see Figure 7.33) consists of 4 p-type transistors and 6 n-type transistors, with two read lines and two write lines. Here, the write access transistors are p-type and the bit lines corresponding to write operation are always connected to V_{DD}. Depending upon the data to be written, either P3 or P4 will be turned ON. During hold, the operation appropriate column-based signals will be activated to maintain the data stored [8].



(b)

Signal	Write "1"	Write "0"	Read	Hold
WLL	GND	VDD	VDD	VDD
WLR	VDD	GND	VDD	VDD
LEN	GND	VDD	GND	VDD
REN	VDD	GND	GND	VDD
RWL	GND	GND	VDD	GND

Figure 7.33 (a) 10T SRAM cell design; (b) signals during operation [8].

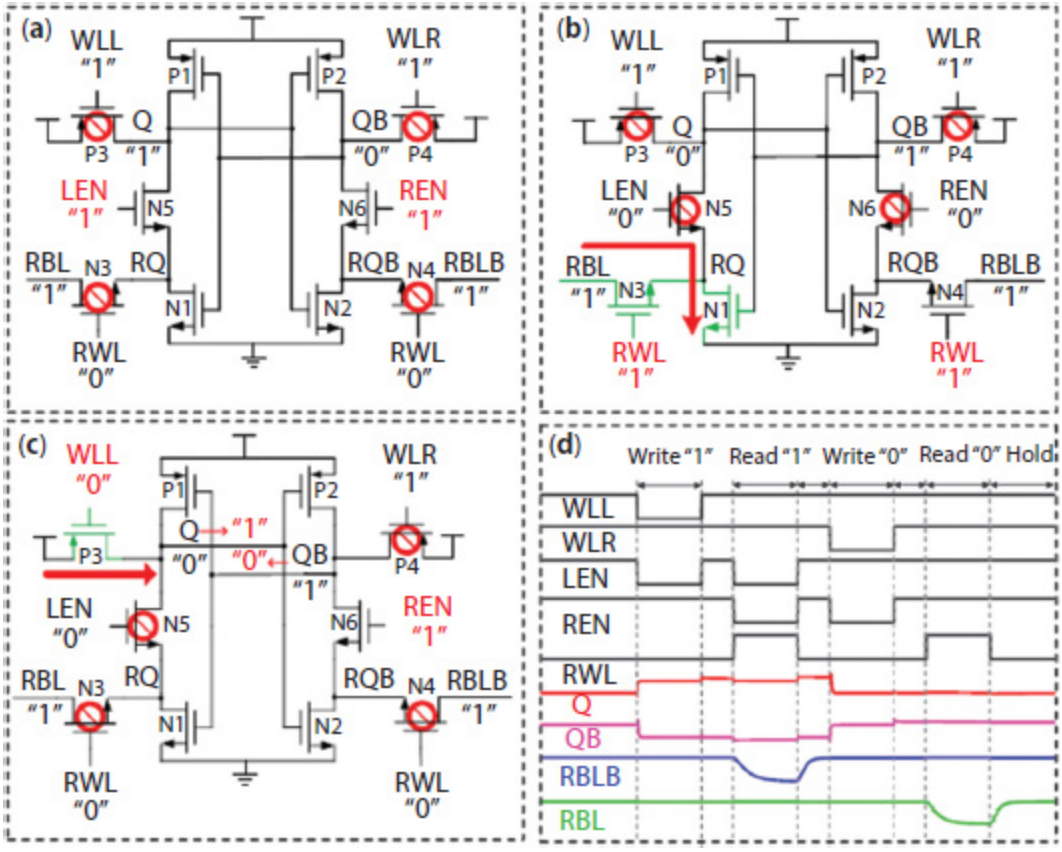


Figure 7.34 (a) Hold state; (b) Read operation; (c) Write operation of Bit "1"; (d) Waveforms during various operating modes [8].

Figure 7.34 illustrates the hold, read operation, and write operation of the proposed 10T SRAM cell using TFET. During the read operation, the read bit lines, RBL, and RBLB are pre-charged to V_{DD}. Then, both the write access transistors are disabled and both read access transistors are enabled. By providing appropriate LEN and REN signals, N5 and N6 are made to be in the off state. Thus, the read path gets separated from the storage nodes and this increases the RSNM. The proposed design was reported to improve the write noise margin also [8].

7.3.5 SRAM Cell Design Based on Negative Differential Resistance Property

Saripalli *et al.* reported a 4T based SRAM cell design by exploiting the negative differential resistance of tunnel FET in the reverse bias condition. A four transistor SRAM cell, which comprises of a latch and two access

transistors, is realized by this group [43]. The 4T SRAM cell circuit is shown in Figure 7.35.

By making use of the negative differential property of tunnel FETs, Navneeth Gupta *et al.* in 2017 reported a 2T1C SRAM. A conventional n-TFET with high k material HfO_2 as gate material is used for the SRAM cell implementation. The circuit of the proposed 2T1C SRAM cell under storing, writing and reading a bit depicted in Figure 7.36, Figure 7.37 and Figure 7.38 respectively below [38].

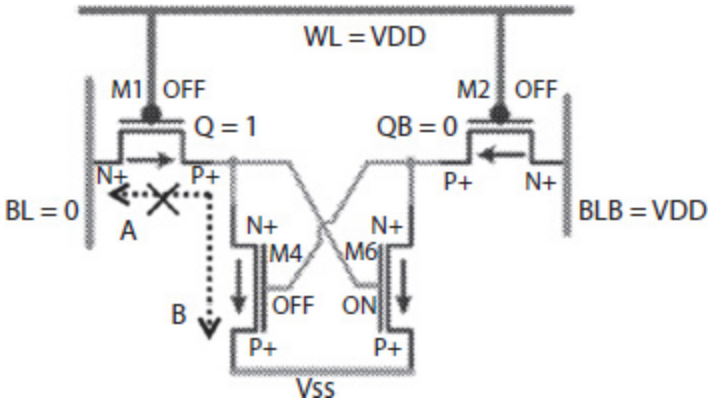


Figure 7.35 4T TFET based SRAM cell [43].

The proposed memory cell offers excellent performance in terms of leakage current compared to the embedded DRAM cell designs and can be identified as a suitable candidate for memory cell implementation with minimum cost [44]. Table 7.5 shows a comparison on the proposed work [44] with the literature [45, 46].

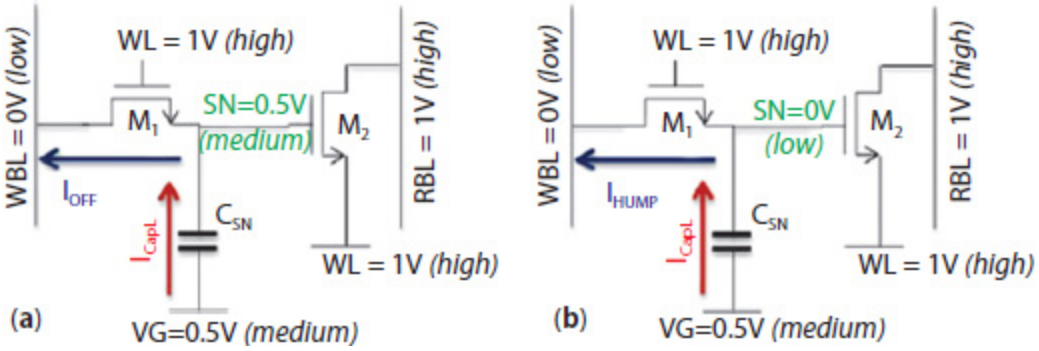


Figure 7.36 Storing the bit [44].

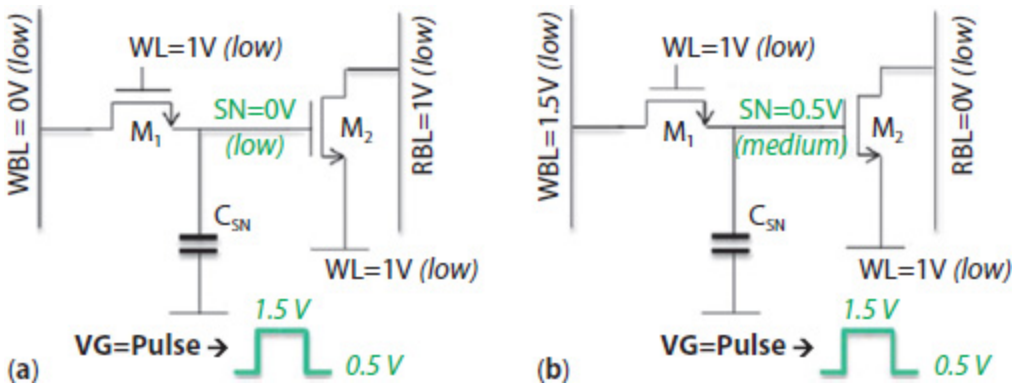


Figure 7.37 Writing the bit [44].

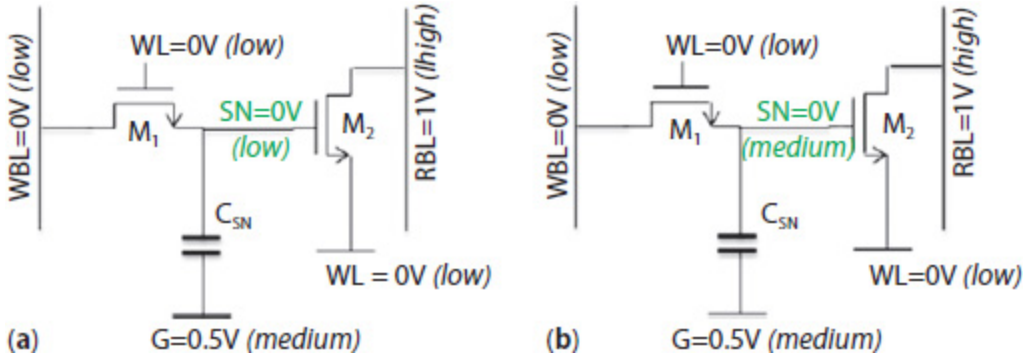


Figure 7.38 Reading a bit [44].

Table 7.5 Comparison of performance parameters of proposed TFET SRAM and other designs in literature [44].

	Proposed SRAM	**Proposed SRAM (Estimation)**	**eDRAM [45]**	**LV SRAM [46]**
Technology	28 nm	22 nm	22 nm	22 nm
Bit Cell Area	0.093 μm^2	< 0.073 μm^2	0.029 μm^2	0.092 μm^2
Refresh Req.	No	No	Yes	No
Retention Time	-	-	100 µs	-
Leakage	<1fA/bit	<1fA/bit	> 100fA/bit	

Navneet Gupta *et al.*, in 2016, reported a low power 3T SRAM cell design by exploring the negative differential resistance property of TFETs [13]. Figure 7.39 depicts the proposed structure in the work [13]. The design makes use of an NDR based 2T-TFET based latch for storing data and 1T for read port. A novel write mechanism using supply lines is put forth in the reported work.

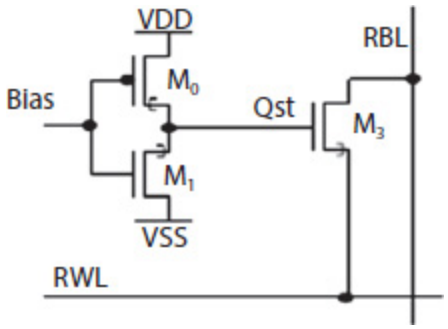


Figure 7.39 Proposed 3T TFET based SRAM cell [13].

7.4 Conclusion

This chapter presents an overview on SRAM cell implementation using TFETs for ultra-low power applications. The shortcomings of conventional tunnel FETs like lower ON current, lower I_{ON}/I_{OFF} ratio, lower subthreshold swing (SS), and characteristics such as ambipolarity, and unidirectionality limits on the read and write abilities of typical 6T SRAM cell implementations. By adopting suitable device engineering approaches and circuit topologies, the performance of the memory cell can be improved. Several optimizations at the architectural level such as double gate, vertical gate, nanowire, and heterostructures were reported in the literature for efficient memory cell designs. TFET based SRAM cells in 6T, 7T, 8T, 9T, and 10T configurations are widely investigated by the research community. In addition, the negative differential resistance property of TFETs is also explored for SRAM cell implementations.

References

1. Zhang, Kevin, ed. *Embedded memories for nano-scale VLSIs*. Vol. 2. New York: Springer, 2009.

2. Park, James J. Jong Hyuk, Victor CM Leung, Cho-Li Wang, and Taeshik Shon. “Future Information Technology, Application, and Service: FutureTech 2012 Volume 2.” (2012).

3. Kumar, Deepak. “Performance evaluation of double gate tunnel FET based chain of inverters and 6-T SRAM cell.” *Engineering Research Express* 1, no. 2 (2019): 025055.

4. Jovanović, Bojan, Raphael M. Brum, and Lionel Torres. “MTJ-based hybrid storage cells for “normally-off and instant-on” computing.” Facta universitatis-series: Electronics and Energetics 28, no. 3 (2015): 465-476.

5. Kang, Sung Mo, and Yusuf Leblebici. CMOS digital integrated circuits. MacGraw-Hill, 2003.

6. Uyemura, John P. CMOS logic circuit design. Springer Science & Business Media, 1999.

7. Singh, Jawar, Krishnan Ramakrishnan, Saurabh Mookerjea, Suman Datta, Narayanan Vijaykrishnan, and D. Pradhan. “A novel Si-tunnel FET based SRAM design for ultra low-power 0.3 V VDD applications.” In *2010 15th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 181-186. IEEE, 2010.

8. Lin, Zhiting, Luanyun Li, Xiulong Wu, Chunyu Peng, Wenjuan Lu, and Qiang Zhao. “Half-select disturb-free 10T tunnel FET SRAM Cell with improved noise margin and low power consumption.” IEEE Transactions on Circuits and Systems II: Express Briefs 68, no. 7 (2021): 2628-2632.

9. Lee, Yoonmyung, Daeyeon Kim, Jin Cai, Isaac Lauer, Leland Chang, Steven J. Koester, David Blaauw, and Dennis Sylvester. “Low-power circuit analysis and design based on heterojunction tunneling transistors (HETTs).” IEEE transactions on very large scale integration (VLSI) systems 21, no. 9 (2013): 1632-1643.

10. Yang, Xuebei, and Kartik Mohanram. “Robust 6T Si tunneling transistor SRAM design.” In 2011 Design, Automation & Test in Europe, pp. 1-6. IEEE, 2011.

11. Strangio, Sebastiano, Pierpaolo Palestri, David Esseni, Luca Selmi, Felice Crupi, Simon Richter, Qing-Tai Zhao, and Siegfried Mantl. “Impact of TFET unidirectionality and ambipolarity on the performance of 6T SRAM cells.” IEEE Journal of the Electron Devices Society 3, no. 3 (2015): 223-232.

12. Chen, Yin-Nien, Ming-Long Fan, Vita Pi-Ho Hu, Pin Su, and Ching-Te Chuang. “Evaluation of stability, performance of ultra-low voltage MOSFET, TFET, and mixed TFET-MOSFET SRAM cell with write-assist circuits.” IEEE Journal on Emerging and Selected Topics in Circuits and Systems 4, no. 4 (2014): 389-399.

13. Gupta, Navneet, Adam Makosiej, Andrei Vladimirescu, Amara Amara, and Costin Anghel. “Ultra-compact SRAM design using TFETs for low power low voltage applications.” In 2016 IEEE international symposium on circuits and systems (ISCAS), pp. 594-597. IEEE, 2016.

14. Luong, Gia Vinh, S. Strangio, A. T. Tiedemann, P. Bernardy, S. Trellenkamp, P. Palestri, S. Mantl, and Q. T. Zhao. “Strained silicon complementary TFET SRAM: Experimental demonstration and simulations.” IEEE journal of the Electron Devices Society 6 (2018): 1033-1040.

15. Ahmad, Sayeed, Naushad Alam, and Mohd Hasan. “Robust TFET SRAM cell for ultra-low power IoT applications.” AEU-International Journal of Electronics and Communications 89 (2018): 70-76.

16. Saurabh, Sneh, and Mamidala Jagadesh Kumar. Fundamentals of tunnel field-effect transistors. CRC press, 2016.

17. Jacobson, Zachery A. Band-to-Band Tunneling Transistors: Scalability and Circuit Performance. University of California, Berkeley, 2012.

18. Narang, Rakhi, Manoj Saxena, R. S. Gupta, and Mridula Gupta. “Device and circuit level performance comparison of tunnel FET architectures and impact of heterogeneous gate dielectric.” JSTS: Journal of Semiconductor Technology and Science 13, no. 3 (2013): 224-236.

19. Seabaugh, Alan C., and Qin Zhang. “Low-voltage tunnel transistors for beyond CMOS logic.” Proceedings of the IEEE 98, no. 12 (2010): 2095-2110.

20. Ahmad, Sayeed, Syed Afzal Ahmad, Mohd Muqeem, Naushad Alam, and Mohd Hasan. “TFET-based robust 7T SRAM cell for low power application.” IEEE Transactions on Electron Devices 66, no. 9 (2019): 3834-3840.

21. Liu, Jheng-Sin, Michael B. Clavel, and Mantu K. Hudait. “An energy-efficient tensile-strained Ge/InGaAs TFET 7T SRAM cell architecture for ultralow-voltage applications.” *IEEE Transactions on Electron Devices* 64, no. 5 (2017): 2193-2200.

22. Chen, Yin-Nien, Ming-Long Fan, Vita Pi-Ho Hu, Pin Su, and Ching-Te Chuang. “Design and analysis of robust tunneling FET SRAM.” *IEEE transactions on electron devices* 60, no. 3 (2013): 1092-1098.

23. Kumar, Parveen, and Sanjeev Kumar Sharma. “Comparative analysis of nanowire tunnel field effect transistor for biosensor applications.” Silicon 13, no. 11 (2021): 4067-4074.

24. Strangio, Sebastiano, Pierpaolo Palestri, David Esseni, Luca Selmi, and Felice Crupi. “Analysis of TFET based 6T SRAM cells implemented with state of the art silicon nanowires.” In 2014 44th European Solid State Device Research Conference (ESSDERC), pp. 282-285. IEEE, 2014.

25. Mohammed, Mahmood Uddin, and Masud H. Chowdhury. “Reliability and energy efficiency of the tunneling transistor-based 6T SRAM cell in sub-10 nm domain.” IEEE Transactions on Circuits and Systems II: Express Briefs 65, no. 12 (2018): 1829-1833.

26. H. Fujiwara, S. Okumura, Y. Iguchi, H. Noguchi, H. Kawaguchi, and M. Yoshimoto, “A 7T/14T dependable SRAM and its array structure to avoid half selection,” in Proc. Int. Conf. VLSI Design, Jan. 2009, pp. 295–300.

27. M. Iijima, K. Seto, M. Numa, A. Tada, and T. Ipposhi, “Improved write margin for 90 nm SOI-7T-SRAM by look-ahead dynamic threshold

voltage control," in Proc. Midwest Symp. Circuits Syst., Aug. 2007, pp. 578–581.

28. S. A. Tawfik and V. Kursun, "Low power and robust 7T dual-Vt SRAM circuit," in Proc. Int. Symp. Circuit Syst., May 2008, pp. 1452–1455

29. L. Chang, D. M. Fried, J. Hergenrother, J. W. Sleight, R. H. Dennard, R. K. Montoye, L. Sekaric, S. J. McNab, A. W. Topol, C. D. Adams, K. W. Guarini, and W. Haensch, "Stable SRAM cell design for the 32 nm node and beyond," in Proc. Symp. VLSI Circuits Dig. Tech. Papers, 2005, pp. 128–129.

30. K. Takeda, Y. Hagihara, Y. Aimoto, M. Nomura, Y. Nakazawa, T. Ishii, and H. Kobatake, "A read-static-noise-margin-free SRAM cell for lowVDD and high-speed applications," IEEE J. Solid-State Circuits, vol. 41, no. 1, pp. 113– 121, Jan. 2006.

31. Saripalli, Vinay, Suman Datta, Vijaykrishnan Narayanan, and Jaydeep P. Kulkarni. "Variation-tolerant ultra low-power heterojunction tunnel FET SRAM design." In *2011 IEEE/ACM International Symposium on Nanoscale Architectures*, pp. 45-52. IEEE, 2011.

32. Chang, Leland, David M. Fried, Jack Hergenrother, Jeffrey W. Sleight, Robert H. Dennard, Robert K. Montoye, Lidija Sekaric *et al.* "Stable SRAM cell design for the 32 nm node and beyond." In Digest of Technical Papers. 2005 Symposium on VLSI Technology, 2005., pp. 128-129. IEEE, 2005.

33. Vladimirescu, Andrei, Costin Anghel, Amara Amara, Navneet Gupta, and Adam Makosiej. "Sub-picowatt retention mode TFET memory for CMOS sensor processing nodes." In 2015 6th International Workshop on Advances in Sensors and Interfaces (IWASI), pp. 266-270. IEEE, 2015.

34. Gupta, Navneet, Adam Makosiej, Oliver Thomas, Amara Amara, Andrei Vladimirescu, and Costin Anghel. "Ultra-low leakage sub-32nm TFET/ CMOS hybrid 32kb pseudo DualPort scratchpad with GHz speed for embedded applications." In 2015 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 597-600. IEEE, 2015.

35. Patnala, Mounica, Avinash Yadav, John Williams, Anoop Gopinath, Brian Nutter, Trond Ytterdal, and Maher Rizkalla. “Low power-high speed performance of 8T static RAM cell within GaN TFET, FinFET, and GNRFET technologies–A review.” Solid-State Electronics 163 (2020): 107665.

36. Gopinath Anoop. Low-Power Hybrid TFET-CMOS Memory. Indianapolis: Purdue University; 2018

37. Boopathi Raja G, Madheswaran M. Performance comparison of GNRFET based 6T SRAM cell with CMOS, FinFET and CNTFET technology. Int J Innovat Res Sci Eng 2016.

38. Liu Huichu, Datta Suman, Naryanan Vijaya Krishnan. A steep switching tunnel FET: a promise to extend the energy efficient roadmap for post-cmos digital and analog/ RF applications. International symposium on low power Electronics and Design (ISLPED). 2013.

39. Mounica M, Chandramohan P. Characterization of 8T SRAM cells using 16nm FinFET technology. International conference on signal processing and communication (ICSC). 2016.

40. Kin Young Bok, Kim Yong-Bin, Lombardi Fabrizio, Lee Young Jun. A low power 8T SRAM cell design technique for CNTFET. International SoC design conference, 2008.

41. Hao Lu, Li Wenjun, Yeqing Lu, Fay Patrick, Ytterdal Trond, Seabaugh Alan. Universal charge-conserving TFET SPICE model incorporating gate current and noise. IEEE J Exploratory Solid-state Comput Dev Circuits 2016.

42. L. Yang *et al.*, “Combinational access tunnel FET SRAM for ultra-low power applications,” in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), Florence, Italy, 2018, pp. 1–5.

43. Saripalli, Vinay, Dheeraj Mohata, Saurabh Mookherjea, Suman Datta, and Vijaykrishnan Narayanan. “TFET based 4T memory devices.” U.S. Patent 8,638,591, issued January 28, 2014.

44. N. Gupta, A. Makosiej, A. Vladimirescu, A. Amara and C. Anghel, “Tunnel FET based ultra-low-leakage compact 2T1C SRAM,” 2017 18th International Symposium on Quality Electronic Design (ISQED), 2017, pp. 71-75, doi: 10.1109/ISQED.2017.7918295.

45. Hamzaoglu, Fatih, *et al.* “A 1 Gb 2 GHz 128 GB/s Bandwidth Embedded DRAM in 22 nm Tri-Gate CMOS Technology.” IEEE Journal of Solid-State Circuits 50.1 (2015): 150-157.

46. Karl, Eric, *et al.* “A 4.6 GHz 162Mb SRAM design in 22nm tri-gate, CMOS technology with integrated active V MIN-enhancing assist circuitry.” IEEE International Solid-State Circuits Conference, 2012.

Note

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8
Epitaxial Layer-Based Si/SiGe Hetero-Junction Line Tunnel FETs: A Physical Insight

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Abstract

Modern semiconductor devices have established a new dimension in handheld consumer and healthcare electronics, such as tablet PC, smartphones, and sensors. This requires an electronic device that consumes less power with a minimum supply voltage and off-state leakage current (I_{OFF}) [1]. The reduction in power dissipation becomes essential as CMOS technologies grow. This demands a new transistor-based switch that works at lower operating voltages and maintains a reduced level of leakage current. In this manner, opportunities and challenges emerge from quantum mechanical transport. A novel tunnel transistor can essentially operate at significantly lower voltages than MOSFETs by employing band-to-band tunneling as the primary conduction mechanism with small subthreshold slopes (SS) [2].

***Keywords*:** Band-to-band tunneling, point & line tunnel FETs, epitaxial engineering, analytical modeling, analog/digital circuit design

8.1 Fundamental Limitation of CMOS: Tunnel FETs

A reduction in the power consumption of MOSFETs is primarily because of the lowering of the supply voltage. However, keeping this trend by employing the CMOS technology scaling gives diminishing results due to an increase in the off-state leakage current. Consequently, the total power consumption also increases. The MOSFET devices suffer from a fundamental limitation of the lower bound o subthreshold slope and thus

also the off-state leakage current. The complementary MOSFETs are unsuitable for circuit operation below 0.5 V supply voltage because of their SS limitation, which is impossible to scale below 60 mV/decade at room temperature, as shown in Figure 8.1(a) [3]. As per the scale length theory of MOSFETs, the threshold voltage can be reduced by the same scale as the supply voltage [4]. This results in a net increase in the gate overdrive voltage and I_{OFF}. Beyond the 65 nm technology node, leakage is very high and static power dominates, as shown in Figure 8.1(b) [5]. Therefore, the fundamental bottleneck with the MOSFET-based technologies is the non-scalability of SS. In conventional MOSFETs, the lower bound of 60 mV/decade is because the subthreshold current is driven by the 'Boltzmann tail' of the source carrier population, with the energies more significant than the top of the barrier in the channel. In addition, this 'Boltzmann tail' becomes more significant because of drain-induced barrier lowering (DIBL), which is a major challenge for the short-channel MOSFETs of the present era.

At room temperature,

$$SS = \frac{dV_{GS}}{dlog_{10}I_D} = \frac{2.3mK_BT}{q} \text{ and } m = 1 + \frac{C_{DEP}}{C_{OX}} \quad (8.1)$$

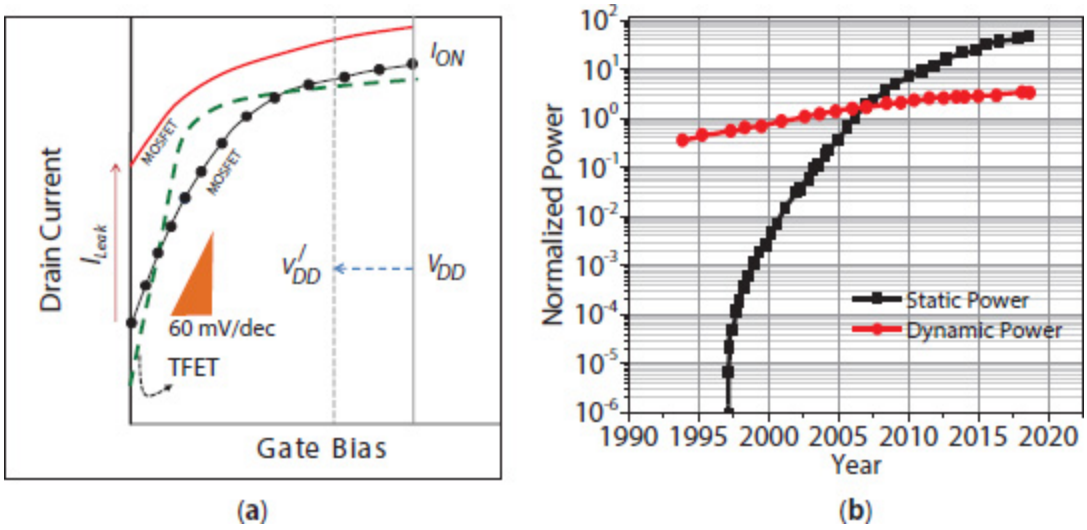

Figure 8.1 (a) Transfer characteristics of MOSFET indicating an exponential increase in the leakage current with a decrease in the threshold voltage (V_{TH}) due to the technology scaling. (b) Trends of dynamic and static CMOS power show that static power consumption has become a serious problem [5].

Equation 8.1 indicates the voltage drop across the channel effectively. Here, m, K_B, T, C_{DEP}, and C_{OX} are the mass of the electron, temperature, Boltzmann's constant, depletion, and oxide capacitance, respectively. This fundamental limitation necessitates a minimal supply voltage for operating the MOSFET devices. In addition, the voltage scaling also hampers the increased variability of the scaled devices owing to the random dopant fluctuations [6].

To prevail over these fundamental constraints, a new carrier injection mechanism must be employed instead of the drift and diffusion of carriers. This has initiated research on so-called "steep slope" transistors which can have SS < 60 mV/decade. Therefore, achieving a good ION/IOFF ratio at lower voltages is possible. Many devices have been proposed to achieve the steep slopes [6]:

- ***Impact Ionization MOS (IMOS)*** is based on the avalanche breakdown principle and requires a high reverse bias voltage.
- ***Nano-Electro-Mechanical Switches (NEMS)*** are fabricated with mechanical contacts. The gate electrode remains in contact with the gate dielectric during the OFF state.

- ***Negative Capacitance FETs (NCFETs)*** are based on the ferroelectric concept.
- ***Hyper FET*** is a recent addition to the plethora of steep slope devices known as Phase Transition FET.
- ***Tunnel FETs*** are based on the band-to-band tunneling transport mechanism and exhibit steep turn-on characteristics. This device will be discussed in the rest of the thesis comprehensively. The above-mentioned steep slope devices are helpful in analog applications to realize:
  - Shorter discharging time for a node capacitor
  - Better analog switch with linear ON state resistance having a lower value
  - Differential amplifier with more significant voltage amplification for small signal
  - Current mirror with more precise current transfer

Among all these devices, band-to-band tunneling (BTBT) transistors have emerged as one of the most promising devices because of their potential for low-voltage operation and fabrication compatibility with CMOS technology [7].

8.2 Working Principle of Tunnel FET

In essence, TFET works as a gated *p*-*i*-*n* structure where the carrier transport takes place by BTBT between the source and channel, as shown in Figure 8.2 [2]. In order to remain consistent with the MOSFET technology, the terminals' names are selected so that the voltages are applied analogously for TFET operation. The n^+ region of TFET is denoted as its drain and the source comprises the p^+ region for an *n*-type device. For an *n*-type device to be in the off-state, the conduction band energy of the channel is higher than the valence band energy of the source, preventing tunneling from occurring [Figure 8.2]. With the high gate bias, the conduction band edge of the channel is pulled below the valence band edge of the source so that BTBT occurs and the device is turned on. Similarly, the *p*-type device

can be realized by just reversing the doping polarity of the *n*-type device. The carrier injection from the source is a strong function of the range of energies over which tunneling can occur. Besides, the high-energy Boltzmann tail of the source distribution does not append to the tunneling current at the low bias.

Therefore, theoretically, TFETs can attain subthreshold swings appreciably below $ln(10)K_BT/q$ mV/decade with a lower value of I_{OFF} [8]. The tunneling probability, T, and tunneling current, I_{BTBT}, can be calculated using the WKB approximation as:

$$I_{BTBT} \propto T \approx \exp\left(\frac{-4\lambda\sqrt{2m^*}Eg^{3/2}}{3\hbar(\Delta\Phi + Eg)}\right) \tag{8.2}$$

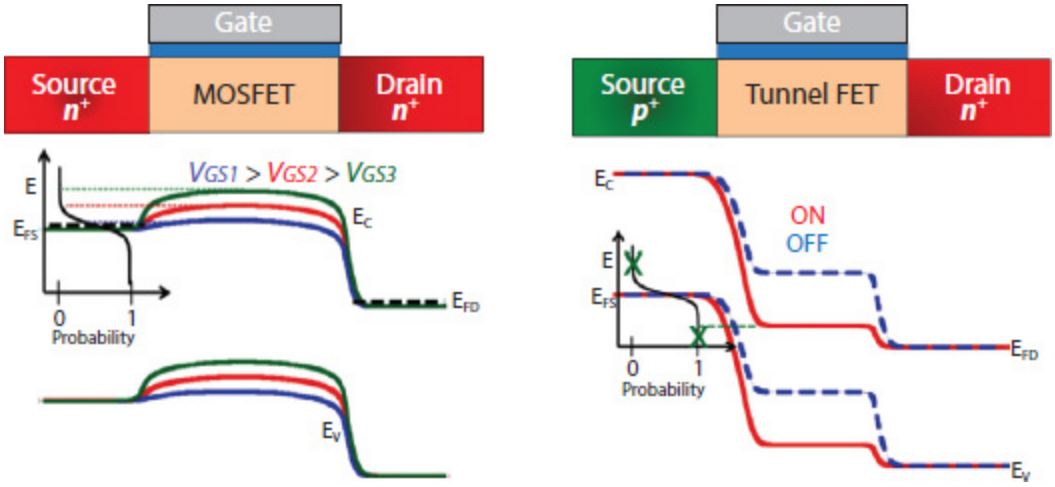

Figure 8.2 Comparison of working mechanism between MOSFET and TFET. E_C, E_V, and E_F are the conduction band, valence band, and Fermi energy, respectively.

Here, E_g is the energy bandgap at the tunnel junction, λ is the screening length, m^* is the tunneling mass, and $\Delta\Phi$ is the range of energy over which tunneling can occur. Therefore, the essential conditions for the band-to-band tunneling to take place are:

- Available states to tunnel from
- Available states to tunnel to

- An energy barrier that is sufficiently narrow for the tunneling to take place
- Conservation of momentum.

Tunnel FETs suffer from low drive currents despite their steep slope. Further, the steep slope also depends on tunneling junctions' interface quality.

8.3 Point and Line TFETs: Tunneling Direction

The research community is extensively researching the steep subthreshold characteristics of tunneling FETs for ultra-low power VLSI design applications [1]-[3]. However, the major challenge for TFETs is their poor drive capability. Thanks to splendid advancements in junction and material engineering, the drive current of TFETs has improved significantly [4]-[6]. Tunnel FETs can be classified into two categories according to tunneling direction. The first one is Point TFET, where tunneling occurs at the edge of the source-channel junction. The contribution of this tunneling is dominant in a small-localized area. The second category is the Line TFET in which the directional of tunneling is orthogonal or perpendicular to the gate, as shown in Figure 8.3.

Line TFETs exhibit one dimensional nature of band-to-band tunneling, unlike point tunneling, where the two-dimensional picture of band-to-band tunneling is present. Line TFETs have an increased area of the cross-section for tunneling. Hence, the driving capability of such devices is always higher than its point tunneling counterparts. The epitaxial layer/ source pocket-based line tunneling FETs are also gaining interest, whereby the source region is overlapped by the metal gate [7]-[11]. Thus, the area of the cross-section for BTBT can be increased. Hence, the drain current will likewise increase, as shown in Figure 8.4. Together with the tunneling probability, the Fermi-Dirac distribution-based occupancy function is equally important in calculating the tunneling current [12]. Recently, the potential of L-TFETs for Internet of Things (IoT) applications has also been verified [13].

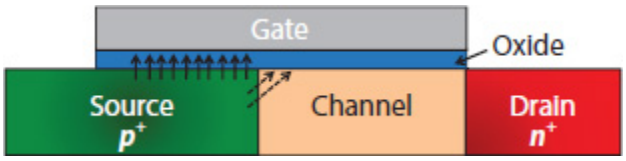

Figure 8.3 Classification of TFETs per direction of tunneling. Solid arrows indicate line tunneling and dashed arrows indicate point tunneling.

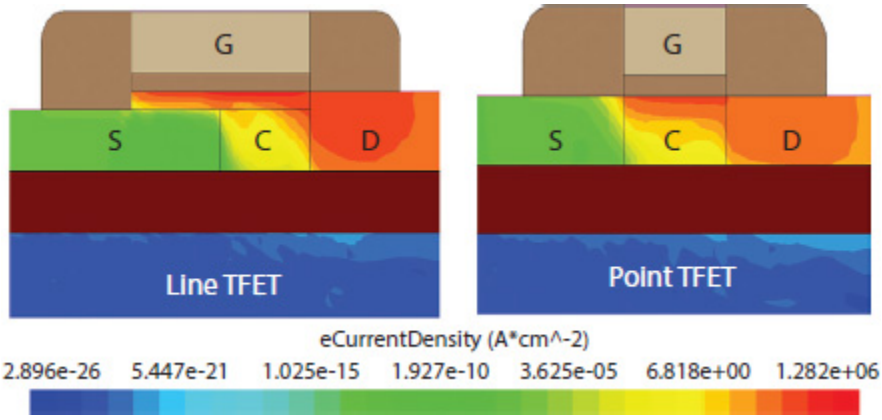

Figure 8.4 Current density in line and point TFET devices obtained through numerical TCAD simulation of two devices.

It is observed from numerical TCAD simulations that the current flow lines are similar for these two devices. However, the current density is higher in the case of Line TFET devices due to the increased cross-section area for tunneling, as shown in Figure 8.4.

8.4 Perspective of Line TFETs

The concept of line TFET was first coined by Vandenberghe *et al.* in 2007 [14]. Thereafter, several researchers successfully demonstrated the fabrication of line TFET devices. Initial demonstrations were based on the gate over source structures. However, the drive capability was not per the requirements of the semiconductor industry. This was due to the delay in the onset of gate normal tunneling. This happens as the band-to-band tunneling takes place for higher gate bias in the gate over the source structures when there is no epitaxial layer or source pocket, as shown in Figure 8.3. In such structures, the gate strictly controls the electrostatic potential of the source region underneath the gate. Therefore, the drain's influence over the source region's electrostatic potential is insignificant.

Contrary to this, the impact of the drain on the point TFET is notable. Thus, the tunneling probability is easily modified by the drain potential in point TFET devices. In most initial analytical models of line TFETs, the impact of the drain over the source electrostatic potential was neglected.

8.4.1 Planar Line Tunnel FETs

An experimental demonstration of L-TFET was given by Zaho *et al.* in 2011 and they did not used any source pocket to enhance the drive capability [15]. However, they used an Si/SiGe hetero-junction to boost the device's performance, as depicted in Figure 8.5(a). The tensile and compressive strains in *Si* and *SiGe* were used respectively to reduce the bandgap to increase the drain current. A valence band offset at the *Si/SiGe* hetero-junction is indicated in Figure 8.5 (b). This should be considered in the numerical simulation to get accurate results. The transfer curves with a steep slope are shown in Figure 8.5(c). The SS of conventional MOSFETs reduces linearly with the temperature. However, line TFET shows different temperature dependence from the MOSFET [Figure 8.5(d)].

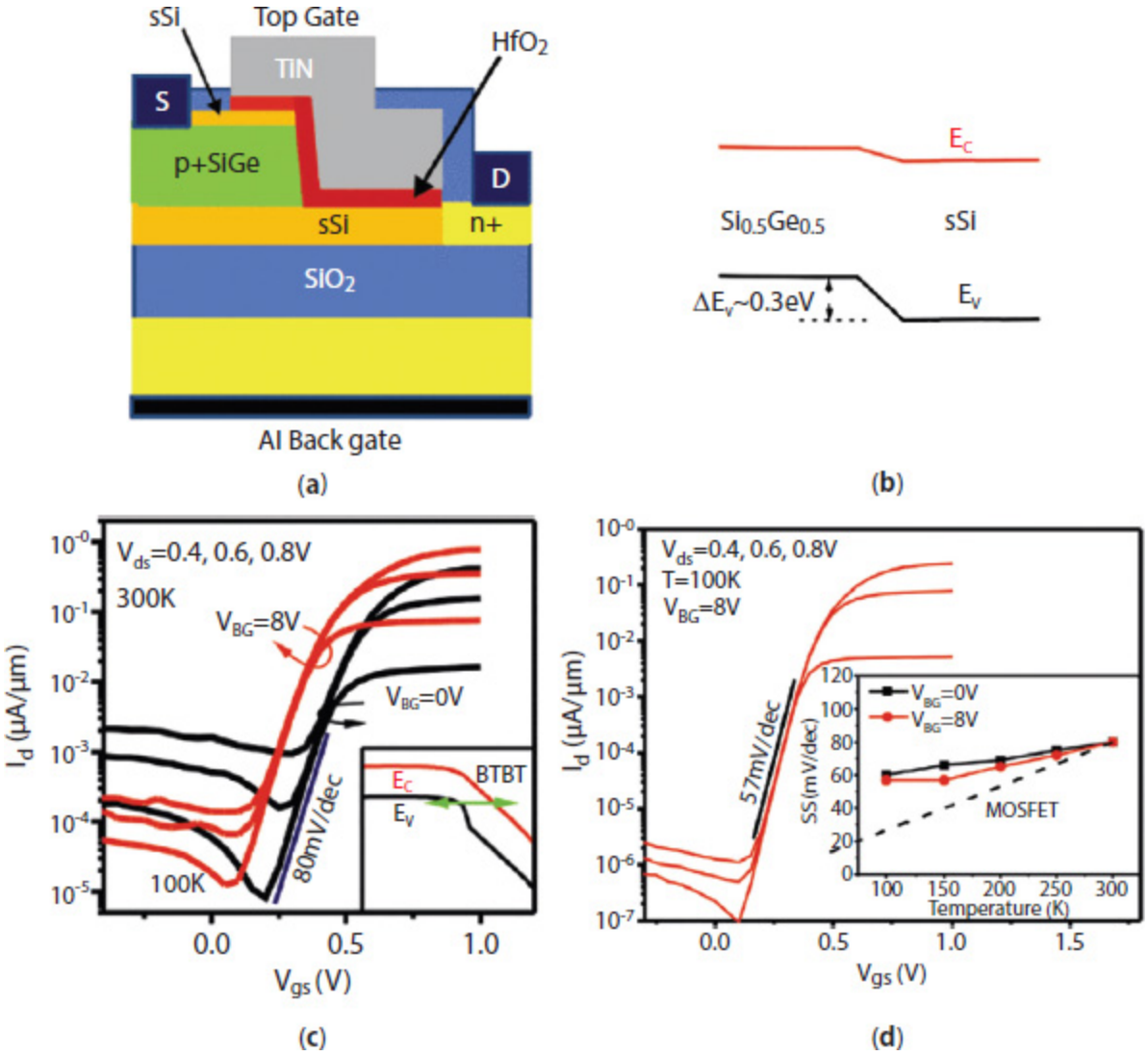

Figure 8.5 (a) Structure of fabricated L-TFET; (b) Energy band offset at hetero-junction; (c) TFET transfer characteristics measured at room temperature under different bias Conditions; (d) Transfer curves measured at 100 K; (d) SS measured at low temperatures [15].

The advancement in junction engineering has significantly improved the drive current of tunnel FETs [16]-[22]. The main enablers are the presence of source pocket and epitaxial layer-based structures to increase the cross-section area for band-to-band tunneling. Recently, the potential of hetero-junction line tunnel FETs (L-TFETs) for analog circuits and Internet of Things (IoT) applications has also been discussed [23]-[25]. Kao *et al.* have demonstrated that the sensitivity to gate alignment and physical oxide thickness are the main disadvantages of L-TFETs, which can be mitigated

by using source pocket/epitaxial layers in L-TFETs [26]. The impact of pocket thickness and doping on the device's electrical characteristics is indicated in Figure 8.6 for different quantum mechanical directions.

Walke *et al.* have successfully fabricated an epitaxial layer-based L-TFET for better drive capability, as shown in Figure 8.7 (a). A hetero-junction between the Silicon epitaxial layer and Silicon-germanium (*SiGe*) sources provides reasonably better electrical characteristics than all Silicon devices [27]. Field Induced Quantum Confinement (FIQC) effects are responsible for the change in the onset of tunneling voltage. In conventional TCAD tools (viz Sentaurus, Atlas, etc.), one has to incorporate the 1-D Schrodinger equation to consider these effects across the *Si/SiGe* MOS junction. In such devices, the *germanium* mole fraction does not affect the longitudinal effective mass of strained *silicon* on *SiGe* [28].

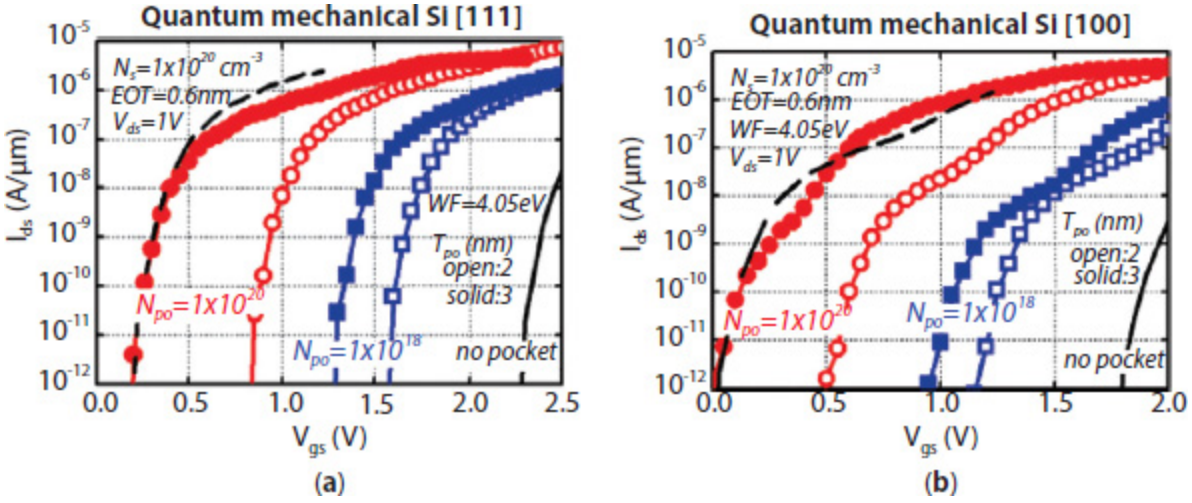

Figure 8.6 Transfer characteristics of counter-doped source pocket-based L-FETs for quantum mechanical tunneling in (a) [111] direction and (b) [100] direction [26].

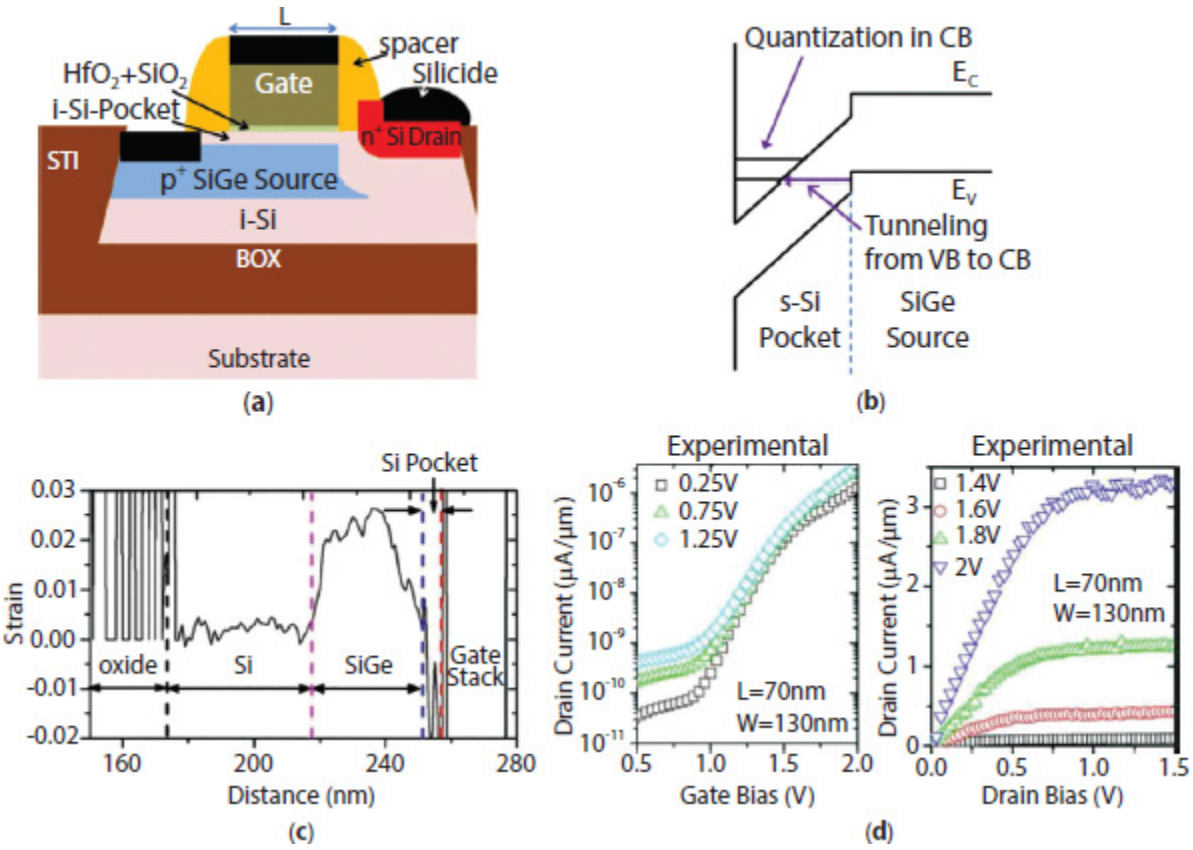

Figure 8.7 (a) 2-D schematic of fabricated device; (b) Band offset at Hetero-junction; (c) Strain profile at source-epitaxial layer; (d) Transfer characteristics [19].

Further, the strained epitaxial layer is considered in most experimental devices, whereas the SiGe source is considered to be relaxed. Several researchers noted tensile strain at the tunneling cross-section in these devices. Here, it is important to note that the FIQC will also affect the sensitivity to the epitaxial layer thickness. However, these effects may be neglected at the Si/SiGe hetero interface in the presence of epitaxial layers of more than 2nm [29]-[30]. Epitaxial layer engineering is the most critical parameter in area-scaled line TFETs. The thickness and doping of these layers can significantly modulate the device's performance.

8.4.2 3D Line TFETs

In recent years, fin-shaped and nanosheet-based line TFETs have been successfully demonstrated for ultra-low power applications [31]-[32]. These devices are promising candidates for sub-10 nm technology nodes. Both

devices employ area-scaled tunneling by using epitaxial layers over the source region. In addition, better electrostatic control of the gate over the tunneling junction will give promising subthreshold swings. The cross-sectional view of the Fin-shaped area scaled line TFET is shown in Figure 8.8(a). Here, the tunneling cross-section is surrounded by the gate in three directions. The device can be fabricated using dummy gate stack deposition and spacer formation, as shown in Figure 8.8(b).

Further, the epitaxial growth process can be used to realize the device. The transfer characteristics for different source doping profiles is shown in Figure 8.8(c). This demonstrates that higher source doping will result in higher OFF state leakages. Therefore, source engineering is also a critical design parameter in line TFET design. The epitaxial layer thickness of less than 2nm severely degrades mobility due to increased scattering [33].

Nanowire Tunnel FETs have been discussed for lateral (point) tunneling by several researchers [34]-[35]. The role of work-function engineering is very important in such devices to understand the modulation of tunneling currents [36]. However, as explained in Section 8.3, the lateral tunneling in *Si/SiGe*-based devices is not per the requirements of the technology roadmap. Further, mass-scale manufacturing for III-V Tunnel FET is not an economically viable solution. Therefore, the epitaxial layer-based line TFET is required to improve the drive capability of Nanowire/Nanosheet transistors for sub-10 nm technology nodes.

The device depicted in Figure 8.9 uses the Nanosheet transistor with epitaxial layer-based line tunneling. Due to the gate-all-around structure, a reasonably good amount of tunneling can be obtained in such devices. The cross-sectional view of the device is shown in Figure 8.9 (c)-(d). By increasing the gate-source overlap, the area of the tunneling cross-section can be increased. The transfer characteristics of such devices exhibit significant improvement in the subthreshold swing, as shown in Figure 8.9 (b). The device design guideline indicates that an epitaxial layer thickness (t_{EPI}) of 3-4 nm is sufficient for improved electrical performance. For $t_{EPI} \leq$ 2 nm, there will not be any significant band bending at the valance band of the source and conduction band of the epitaxial layer for tunneling to happen. Therefore, the thickness optimizes around 3-4 nm for such devices for suitable doping value. Thus, the epitaxial (nEPI) layer doping is also a

critical design parameter. The increase in n_{EPI} results in higher drive current as well as leakage current. Therefore, the optimum doping is around 1×10^{18} cm^{-3}. The drain current initially increases linearly with the gate-source overlap length (L_{OV}), then a sub-linear increase is observed in such devices. This is due to high channel resistance at higher L_{OV} values.

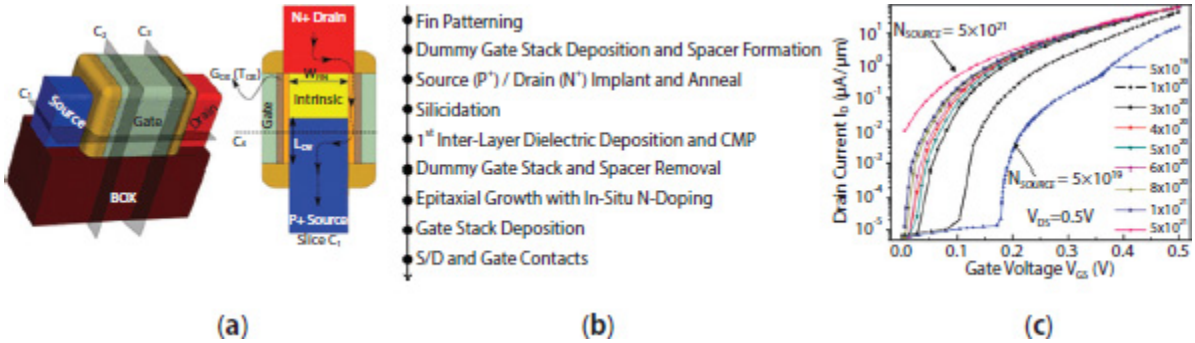

Figure 8.8 3D/2D cross-section of Fin-shaped line tunnel FET; (b) Typical process flow for device; (c) Corresponding transfer characteristics [31].

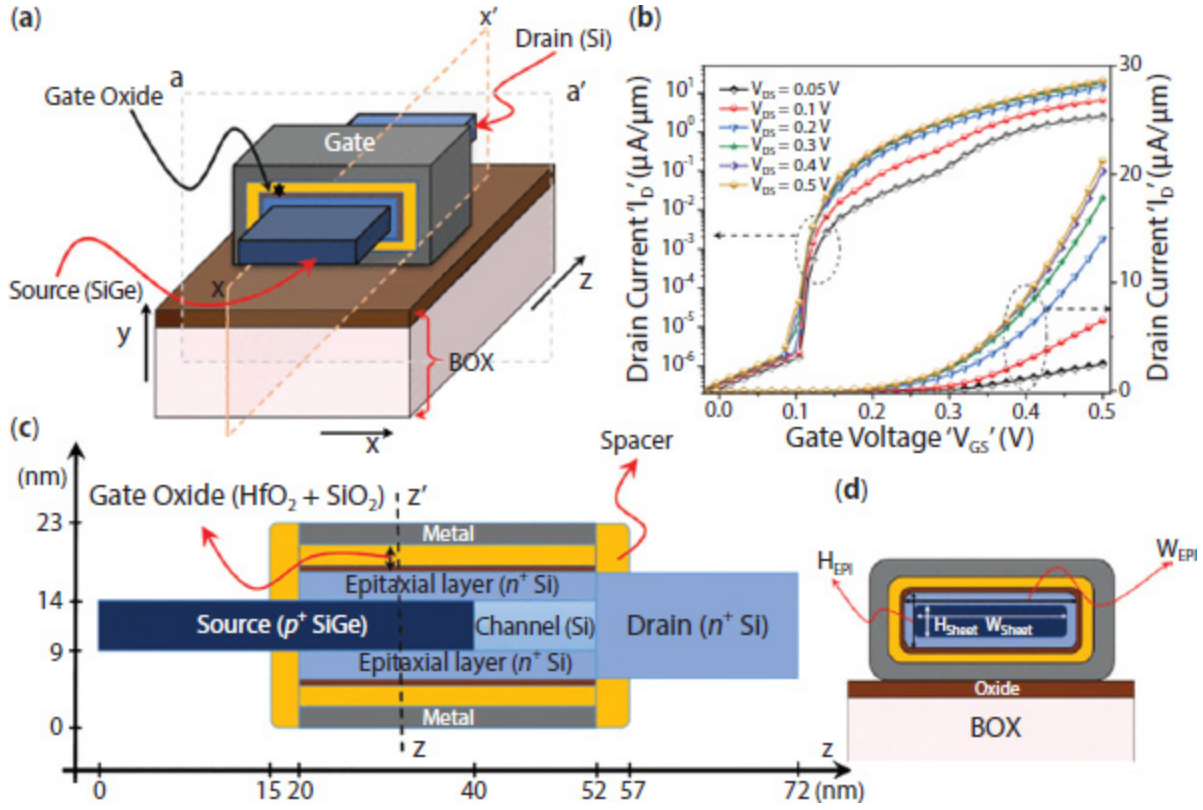

Figure 8.9 (a) Three-dimensional schematic of area-scaled NS-TFET; (b) Transfer characteristic of device under consideration (note that the current is normalized against the effective width $W_{eff} = 2H_{sheet}+2W_{sheet}$); (c) 2-D slice of (a) along channel's x –x′ plane showing Epi-overlap region over source and channel; and (d) 2-D slice of (a) Across channel's a -a′ plane showing Epi-layer over source [32].

Further, the stacking of Nanosheets will improve such devices' drive capability, as shown in Figure 8.10. The vertical stacking of multiple Nanosheets does not require any additional footprint area [37]. In Nanosheets, an epitaxial layer is grown over the source, as shown in the cross-section along the z-plane of Figure 8.10 (a). The corresponding improvement (~3×) in drain current and subthreshold slope is also depicted in Figure 8.10(b). Although self-heating is an important concern for stacked Nanosheet transistors, the area scaled line TFETs are thermally cooler than their MOSFET counterparts due to BTBT as the main carrier transport mechanism.

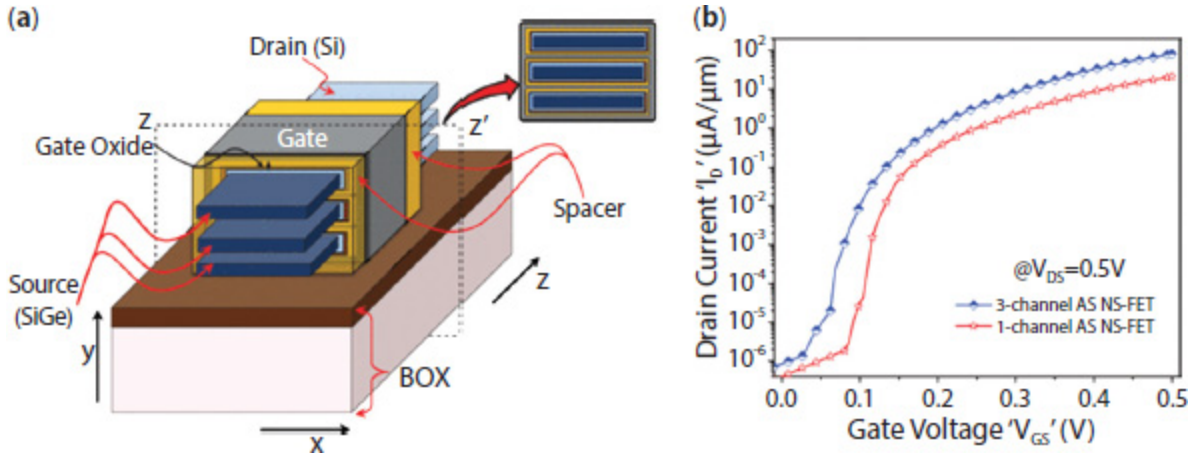

Figure 8.10 (a) Stacked nanosheet line TFET with 3 sheets; (b) Cross-section along z plane and transfer characteristics of target device.

8.5 Analytical Models of Line TFETs

Several compact analytical models for TFETs have been proposed in the last decade. However, few of them are for line TFETs [38]. The drain current for point TFET is expressed as follows [39]:

$$I_D \approx \overline{P}_{Kane} \exp\left(-B_{Kane} q \sqrt{E_g} l_{path}\right) dV \tag{8.3}$$

Here, $\overline{P}_{Kane}$ is the modified prefactor, E_g is the energy bandgap, B_{Kane} is the material dependent constant, and l_{path} is the length of the tunnel path. This equation can be used for a single gate, double gate, and nanowire TFETs to estimate the drive capability. Vandenberghe *et al*. [40] have proposed a compact analytical model for line TFET without an epitaxial layer and source pockets. The tunneling current is calculated with Kane's model, as follows [45]:

$$I_D \approx \frac{WLAE_g^{D-1}}{2Bq^D}\left(\frac{1}{l_{path}^D} - \frac{2E_g\epsilon_S}{q^2 N_a}\frac{1}{l_{path}^{D+2}}\right)\exp\left(-B_{Kane} q \sqrt{E_g} l_{path}\right) \tag{8.4}$$

Here, L and W are length and width, respectively. Kane's model parameter B depends upon the effective mass of the conduction/valence band and D is a fitting constant. Recently, the compact analytical model for epitaxial layer-based Line TFET is also presented [41]-[42]. This model is based on

the surface electrical potential calculation. This can be calculated by knowing the values of length (λ) and inversion charge density (N_{inv}) per gate length. Finally, the local electrical field (E_{local}) is calculated to determine the tunneling rate with Kane's model. In order to consider the impact of the gate and drain bias on the tunneling, the Fermi Dirac distribution function for the source and epitaxial layer is also considered. The drain current is primarily due to BTBT only, which is given by $I_D = I_{BTBT}$. With this method, the value of I_{OFF} is given by:

$$I_{OFF} = \frac{WqD_n n_i^2}{N_S H_s} + \frac{t_c q D_p n_i^2}{N_D W_D} \tag{8.5}$$

Here, H_S is the source height and N_D and W_D are the drain region's doping and width. D_n and D_p are the diffusion constants for electron and hole, respectively. Also, the term N_S and t_c represent the source doping and channel thickness. This model can also predict the onset of tunneling voltage and the threshold voltage of the device.

Further, the extraction of saturation voltages for Line TFETs is based on the specific value of gate-drain capacitance [43]. The saturation in line TFETs is independent of the gate-source overlap lengths. Thus, the gate-drain capacitances for different gate-source overlap lengths show similar behavior until saturation takes place, as shown in Figure 8.11. The soft saturation in the device is attained at the electron density in the epitaxial layer saturates and deep saturation is attained when it drops below the doping level. The gate-drain bias (V_{GD}) is found to be a constant at the onset of saturation and remains independent of the gate-source overlap lengths. The saturation voltage at the onset of soft and deep saturation is given by $V_{DSAT}^{s,d} = V_{GS} - V_{GD}^{s,d}$. The estimation of V_{GD} and V_{DSAT} is shown in Figure 8.11 (a)-(b).

Line TFETs are promising for circuit design due to the dependence of drive current on the gate-source overlap length. A gate-source overlap aware small signal model of line TFET can be obtained by calculating the drain current of the device [44]. The transconductance increases linearly with the gate-source overlap, whereas the output resistance remains almost independent of the same. Similarly, the gate-drain capacitance remains almost unaltered with overall (L_{OV}). However, the gate-source capacitances

increase almost linearly. The gate-source overlap can be used as a circuit design parameter, similar to the device width. The increase in device width decreases the output resistance, however, it remains the same with an increase in L_{OV}.

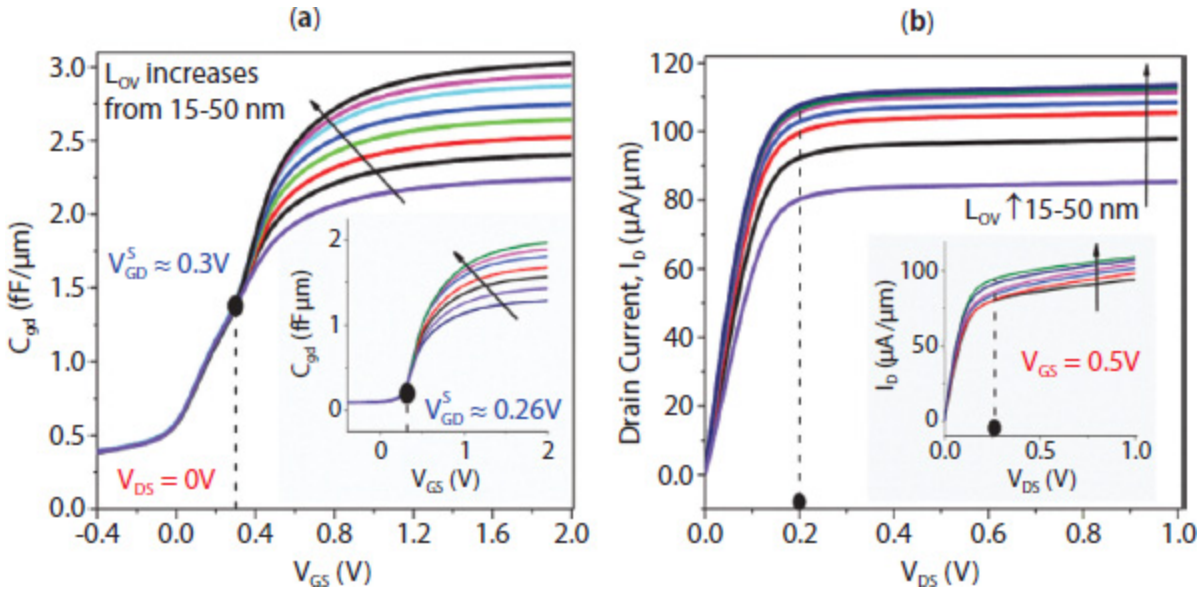

Figure 8.11 (a) Estimating constant gate-drain bias from gate capacitance curve with different gate-source overlaps; (b) Soft saturation indicated in output characteristics.

8.6 Line TFETs for Analog & Digital Circuits Design

TFETs are promising for low-power and low-voltage circuits due to their steep slope and high-output resistance. Successful demonstrations of lateral tunneling-based TFETs for analog and digital applications have been given in the last decade [45]-[47]. Recently, a successful demonstration of Line TFETs for analog and digital circuits has also been proposed by several researchers.

The impact of gate-source overlap length on the performance of Line TFET-based current mirror [Figure 8.12 (a)] is discussed in [48]. The device under consideration is shown in Figure 8.7 (a). This device always outperforms the point TFET and FinFET as far as low-temperature sensitivity is concerned. However, line TFETs are not suitable if the sensitivity to

channel length is the main concern. Due to bandgap narrowing, the current transfer ratio with line TFETs showed a nearly linear relationship on temperature when band-to-band tunneling dominates both input and output transistors of the current mirror circuit, as shown in Figure 8.12 (b).

It has been experimentally demonstrated that the intrinsic gain of line TFET (with an abruptly doped junction) is reasonably better than the MOSFET counterpart due to near-perfect saturation [49]-[50]. Line TFETs can also be used for bio-sensing applications, as the sensitivity of such devices is always better than the point TFETs. The turn-on voltage and sub-thermal swing of line TFET shows more sensitivity to the bio-molecules than MOSFETs.

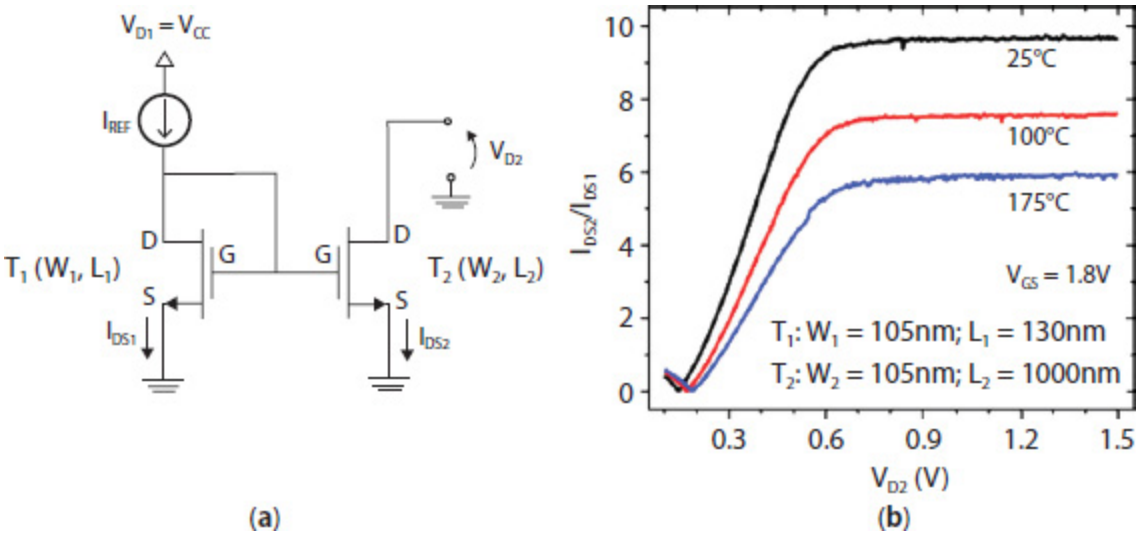

Figure 8.12 (a) Line TFET-based current mirror circuit; (b) Current ratio in input and output transistors [48].

The area-scaled tunnel FET is also a very good alternative for digital circuit design and IoT applications [51]. An experimental demonstration of an FinTFET inverter is recently given with a very small value of short circuit current. A sharp transition in voltage transfer characteristics can be obtained by using line TFETs. The drive current of n/p devices can be adjusted by modifying the number of fins of area scaled FinTFET. Thus, the area-scaled FinTFET inverter is best suited for ultralow-power and lowcost IoT applications.

8.7 Other Steep Slope Devices

Apart from Line/Point Tunnel FETs, some other steep slope devices can be used for data intensive and IoT applications. Brief details of such devices are presented here:

- ***Impact Ionization MOS (IMOS)*** is based on the avalanche breakdown principle and requires a high reverse bias voltage. When the device operates in the saturation regime, the steep slope is achieved by impact ionization in the high-field region (drain junction). The *hole* current generated due to impact ionization (for an *n*-channel device) enhances the potential of the transistor body near the channel region. This decreases the threshold voltage and increases the drive current [52]. The increase in further current increases the rate of impact ionization. Through the process, a positive feedback loop is completed. Consequently, the drain current latches rapidly from the OFF state to the ON state and SS < 60 mV/decade can be observed [53]. However, these devices suffer from serious scalability issues.
- ***Nano-Electro-Mechanical Switches (NEMS)*** are fabricated with mechanical contacts. The gate electrode remains in contact with the gate dielectric during the OFF state, thus, the short-channel effects are efficiently suppressed. In addition, the gate electrode gets separated from the gate dielectric during the ON state. This dynamically lowers the threshold voltage and the drive current of the transistor is enhanced in addition to eliminating the gate leakage. The NEMFETs are likely to meet the performance specifications for the low power applications, even at 25 nm gate length, and are an attractive choice for scaled supply voltage operation [54]. These devices have a lower speed and also suffer from reliability issues.
- ***Negative Capacitance FETs (NCFETs)*** are based on the ferroelectric concept. The concept of NCFET was recently demonstrated by Salahuddin *et al.* in 2008, using a negative differential capacitance [55]. Theoretical NCFET projections were reported using $HfZrO_2$ as anti-ferroelectric material and it was shown that a minimum SS ~ 23 mV/decade could be achieved [56]. NCFETs with ferroelectric and organic material in their gate stack have also been experimentally demonstrated with SS ~ 18 mV/decade [57]. A minimum SS ~ 8.5 mV/decade for a FinFET-based negative capacitance device was

experimentally measured with wide hysteresis [58]. The ferroelectric $HfZrO_x$ FET was experimentally reported with a small hysteresis window shift (<0.1 V), reverse SS ~ 28 mV/dec, and forward SS ~ 42 mV/dec. These devices are primarily used for energy-harvesting applications [59]. It is found that the ferroelectric damping effect results in considerable short-circuit power and delay, which in turn limits high-frequency operation [60]. The ferroelectric thickness should be tuned correctly to get saturated output characteristics. In addition, these devices suffer from lower speed and the interface states also pose fabrication complexity.

- ***Hyper FET*** is a recent addition to the plethora of steep slope devices known as Phase Transition FET. The source terminal is attached to the phase transition correlated material in these devices. The steep slope of the Hyper-FET is due to the collective carrier dynamics of the correlated material. During the transistor operation, these materials experience selective phase switching. The correlated materials show a strong correlation among their inherent electrons. Consequently, they have remarkable electronic and magnetic properties such as spin-charge separation, metal-insulator transitions, and half-metallicity [61]. A few examples of these materials are vanadium dioxide, doped chalcogenide, Cu-doped HfO2, etc., which have highly nonlinear electric behavior. Hyper-FETs' functionalities have been shown experimentally with the transistor's discrete and monolithic incorporation of the correlated material. In addition, SS ~ 8 mV/decade has been measured in the monolithically integrated Hyper-FET [52].

8.8 Conclusion

The epitaxial layer-based line TFETs is far superior to their point TFET counterparts, as the drive capability can be improved by varying the gate-source overlap. This area scaling can also be used in circuit design where gate-source overlap rather than the width can alter the drive capability. The area scaled tunneling can effectively reduce the sub-threshold swing without affecting the OFF current. The drive capability can also be modified by selecting the source's appropriate mole fraction of germanium. The epitaxial engineering is a critical parameter in the device design and

needs to be appropriately optimized for good performance. Thus, the epitaxial layer/source pocket for line tunneling is a very good alternative for future-generation devices.

References

1. Semiconductor Industry Association, International Technology Roadmap for Semiconductors (ITRS), 2015.

2. A. M. Ionescu and H. Riel, “Tunnel field-effect transistors as energy-efficient electronic switches,” Nature, vol. 479, no. 7373, pp. 329–337, 2011.

3. Y. Taur and T. H. Ning, “Fundamentals of modern VLSI devices,” Cambridge University Press, Cambridge, 2013.

4. S. E. Thompson and S. Parthasarathy, “Moore’s law: the future of Si microelectronics,” Materials Today, vol. 9, no. 6, pp. 20-25, 2006.

5. H. Iwai, “Roadmap for 22nm and beyond (Invited Paper),” Microelectron. Eng., vol. 86, no. 7–9, pp. 1520–1528, 2009.

6. S. B. Rahi, and B. Ghosh. “High-k double gate junctionless tunnel FET with a tunable bandgap.” RSC Advances 5, no. 67 (2015): 54544-54550.

7. H. Lu and A. Seabaugh, “Tunnel field-effect transistors: State-of-the-art,” IEEE J. Electron Devices Soc., vol. 2, no. 4, pp. 44–49, 2014.

8. J. Knoch, S. Mantl, and J. Appenzeller, “Impact of the dimensionality on the performance of tunneling FETs: Bulk versus one-dimensional devices,” Solid. State. Electron., vol. 51, no. 4 pp. 572–578, 2007.

9. P.-F. Wang, K. Hilsenbeck, Th. Nirschl, M. Oswald, Ch. Stepper, M. Weis, D. Schmitt-Landsiedel, W. Hansch, “Complementary tunneling transistor for low power application,” Solid. State. Electron., vol. 48, no. 12, pp. 2281–2286, 2004.

10. S. Banerjee, W. Richardson, J. Coleman, and A. Chatterjee, “A New Three-Terminal Tunnel Device,” IEEE Electron Device Lett., vol. 8, no. 8, pp. 347– 349, 1987.

11. T. Baba, “Proposal for Surface Tunnel Transistors,” Jpn. J. Appl. Phys., vol. 31, no. 4, pp. L455–L457, 1992.

12. W. M. Reddick and G. A. J. Amaratunga, “Silicon surface tunnel transistor,” Appl. Phys. Lett., vol. 67, no. 4, pp. 494-496, 1995.

13. J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, “Band-to-band tunneling in carbon nanotube field-effect transistors.,” Phys. Rev. Lett., vol. 93, no. 19, p. 196805, 2004.

14. A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, “Tunnel field-effect transistor without gate-drain overlap,” Appl. Phys. Lett., vol. 91, no. 5, pp. 3102-1, 2007.

15. Q. T. Zhao, J. M. Hartmann and S. Mantl, “An Improved Si Tunnel Field Effect Transistor With a Buried Strained Si1−xGex Source,” in IEEE Electron Device Letters, vol. 32, no. 11, pp. 1480-1482, Nov. 2011, doi: 10.1109/ LED.2011.2163696.

16. S. Blaeser et al., “Novel SiGe/Si line tunneling TFET with high Ion at low Vdd and constant SS,” 2015 IEEE International Electron Devices Meeting (IEDM), 2015, pp. 22.3.1-22.3.4, doi: 10.1109/IEDM.2015.7409757.

17. L. Lattanzio, N. Dagtekin, L. De Michielis, and A. M. Ionescu, “On the static and dynamic behavior of the germanium electron-hole bilayer tunnel FET,” *IEEE Trans. Electron Devices*, vol. 59, no. 11, Nov. pp. 2932–29382012, doi: 10.1109/TED.2012.2211600.

18. I. A. Fischer, A. S. M. Bakibillah, M. Golve, D. Hahnel, H. Isemann, A. Kottantharayil, M. Oehme, and J. Schulze, “Silicon tunneling field-effect transistors with tunneling in line with the gate field,” *IEEE Electron Device Lett*., vol. 34, no. 2, pp. 154–156, Feb. 2013, doi: 10.1109/LED.2012.2228250.

19. A. M. Walke, A. Vandooren, R. Rooyyackers, D. Leonelli, A. Hikavyy, R. Loo, A. S. Verhulst, K.-H. Kao, C. Huyghebaert, G. Groeseneken, V. R. Rao, K. K. Bhuwalka, M. M. Heyns, N. Collaert, and A. V. Y. Thean, “Fabrication and analysis of a Si/$Si_{0.55}Ge_{0.45}$ hetero-junction line tunnel

FET," *IEEE Trans. Electron Devices*, vol. 61, no. 3, pp. 707–715, Mar. 2014, doi: 10.1109/TED.2014.2299337.

20. P.-Y. Wang and B.-Y. Tsui, "Experimental demonstration of P-channel germanium epitaxial tunnel layer (ETL) tunnel FET with high tunneling current and high on/off ratio," *IEEE Electron Device Lett.*, vol. 36, no. 12, pp. 1264–1266, Dec. 2015, doi: 10.1109/LED.2015.2487563.

21. S. W. Kim J. H. Kim T.-J. K. Liu, W. Y. Choi, and B.-G. Park, "Demonstration of L-shaped tunnel field-effect transistors," *IEEE Trans. Electron Devices*, vol. 63 no. 4 pp. 1774-1778 Apr. 2016, doi: 10.1109/TED.2015.2472496.

22. S. Sant and A. Schenk, "Method to enhance the performance of InGaAs/InP hetero-junction tunnel FETs," *IEEE Trans. Electron Devices*, vol. 63, no. 5, pp. 2169–2175, May 2016, doi: 10.1109/TED.2015.2489844.

23. Morita Y, Fukuda K, Liu Y, Mori T, Mizubayashi W, Fuketa H, Otsuka S, Migita S, Masahara M, Endo K, and Ota H, "Tunnel FinFET CMOS inverter with very low short-circuit current for ultralow-power Internet of Things application," *Jpn. J. Appl. Phys*., vol. 56, no. 04, p. 04CD19, Mar. 2017, doi: 10.7567/JJAP.56.04CD19.

24. M. D. V. Martino, J. A. Martino, P. G. D. Agopian, A. Vandooren, R. Rooyackers, E. Simoen, and C. Claey, "Analysis of current mirror circuits designed with line tunnel FET devices at different temperatures," *Semicond. Sci. Technol*., vol. 32, no. 5, pp. 5015-1, 2017, doi: 10.1088/1361-6641/aa6764.

25. H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-art," *IEEE J. Electron Devices Soc*., vol. 2, no. 4, pp. 44–49, 2014, doi: 10.1109/ JEDS.2014.2326622.

26. K. -H. Kao et al., "Optimization of Gate-on-Source-Only Tunnel FETs With Counter-Doped Pockets," in IEEE Transactions on Electron Devices, vol. 59, no. 8, pp. 2070-2077, Aug. 2012, doi: 10.1109/TED.2012.2200489

27. A. M. Walke, W. G. Vandenberghe, K. -H. Kao, A. Vandooren and G. Groeseneken, “A Simulation Study on Process Sensitivity of a Line Tunnel Field-Effect Transistor,” in IEEE Transactions on Electron Devices, vol. 60, no. 3, pp. 1019-1027, March 2013, doi: 10.1109/TED.2013.2242201.

28. E. Ungersboeck, S. Dhar, G. Karlowatz, V. Sverdlov, H. Kosina and S. Selberherr, “The effect of general strain on the band structure and electron mobility of silicon”, IEEE Trans. Electron Devices, vol. 54, pp. 2183-2190, Sep. 2007.

29. A. Rajoriya, M. Shrivastava, H. Gossner, T. Schulz and V. R. Rao, “Sub 0.5 V Operation of Performance Driven Mobile Systems Based on Area Scaled Tunnel FET Devices,” in IEEE Transactions on Electron Devices, vol. 60, no. 8, pp. 2626-2633, Aug. 2013, doi: 10.1109/TED.2013.2270566

30. R. Li, L. Yeqing, Z. Guangle, L. Qingmin, C. S. Doo, T. Vasen, et al., “ AlGaSb/ InAs tunnel field-effect transistor with on-current of 78 \$(mu{rm A}/mu{rm m})\$ at 0.5 V “, IEEE Electron Device Lett., vol. 33, pp. 363-365, Mar. 2012.

31. K. Hemanjaneyulu and M. Shrivastava, “Fin Enabled Area Scaled Tunnel FET,” in IEEE Transactions on Electron Devices, vol. 62, no. 10, pp. 3184-3191, Oct. 2015, doi: 10.1109/TED.2015.2469678.

32. S. Srivastava, S. Panwar and A. Acharya, “Proposal and Investigation of Area Scaled Nanosheet Tunnel FET: A Physical Insight,” in IEEE Transactions on Electron Devices, vol. 69, no. 8, pp. 4693-4699, Aug. 2022, doi: 10.1109/ TED.2022.3184915.

33. R. Asra, K. V. Murali and V. R. Rao, “A binary tunnel field effect transistor with a steep sub-threshold swing and increased on current”, Jpn. J. Appl. Phys., vol. 49, no. 12R, pp. 120203, 2010.

34. Knoch, Joachim. “Nanowire tunneling field-effect transistors.” Semiconductors and Semimetals. Vol. 94. Elsevier, 2016. 273-295.

35. A. Acharya, S. Dasgupta and B. Anand, “A Novel VDSAT Extraction Method for Tunnel FETs and Its Implication on Analog Design,” in

IEEE Transactions on Electron Devices, vol. 64, no. 2, pp. 629-633, Feb. 2017, doi: 10.1109/TED.2016.2635688.

36. N. Thoti, Y. Li and W.-L. Sung, “Significance of work function fluctuations in SiGe/Si hetero-nanosheet tunnel-FET at sub-3 nm nodes”, IEEE Trans. Electron Devices, vol. 69, no. 1, pp. 434-438, Jan. 2022.

37. L. Cai, W. Chen, G. Du, X. Zhang and X. Liu, “Layout design correlated with self-heating effect in stacked nanosheet transistors”, IEEE Trans. Electron Devices, vol. 65, no. 6, pp. 2647-2653, Jun. 2018.

38. D. Esseni, M. Pala, P. Palestri, C. Alper and T. Rollo, “A review of selected topics in physics-based modeling for tunnel field-effect transistors”, Semicond. Sci. Technol., vol. 32, no. 8, Jul. 2017.

39. A. S. Verhulst, B. Soree, D. Leonelli, W. G. Vandenberghe and G. Groeseneken, “Modeling the single-gate double-gate and gate-all-around tunnel field effect transistor”, J. Appl. Phys., vol. 107, no. 2, pp. 024518-1-024518-8, Jul. 2010

40. W. Vandenberghe, A. Verhulst, G. Groeseneken, B. Soree and W. Magnus, “Analytical model for a tunnel field-effect transistor”, Proc. MELECON, pp. 923-928, 2008.

41. Q. Cheng, S. Khandelwal and Y. Zeng, “A Physics-Based Model of Vertical TFET—Part I: Modeling of Electric Potential,” in IEEE Transactions on Electron Devices, vol. 69, no. 7, pp. 3966-3973, July 2022, doi: 10.1109/ TED.2022.3172929.

42. Q. Cheng, S. Khandelwal and Y. Zeng, “A Physics-Based Model of Vertical TFET—Part II: Drain Current Model,” in IEEE Transactions on Electron Devices, vol. 69, no. 7, pp. 3974-3982, July 2022, doi: 10.1109/TED.2022.3146091.

43. A. Acharya, A. B. Solanki, S. Dasgupta and B. Anand, “Drain current saturation in line tunneling-based TFETs: An analog design perspective”, IEEE Trans. Electron Devices, vol. 65, no. 1, pp. 322-330, Jan. 2018.

44. A. Acharya, A. B. Solanki, S. Glass, Q. T. Zhao and B. Anand, “Impact of gate-source overlap on the device/circuit analog performance of line TFETs”, IEEE Trans. Electron Devices, vol. 66, no. 9, pp. 4081-4086, Sep. 2019.

45. B. Sedighi, X. S. Hu, H. Liu, J. J. Nahas, and M. Niemier, “Analog Circuit Design Using Tunnel-FETs,” IEEE Trans. Circuits Syst. I, vol. 62, no. 1, pp. 39–48, 2015.

46. A. Biswas, G. V. Luong, M. F. Chowdhury, C. Alper, Q.-T. Zhao, F. Udrea, S. Mantl, and A. M. Ionescu, “Benchmarking of Homojunction Strained-Si NW Tunnel FETs for Basic Analog Functions,” IEEE Trans. Electron Devices, vol. 64, no. 4, pp. 1441–1448, 2017.

47. D. Esseni and M. Alioto, “Device-circuit co-design and comparison of ultralow voltage Tunnel-FET and CMOS digital circuits,” in Proceedings of the International New Circuits and Systems Conference, 2014, pp. 321–324.

48. M. D. V. Martino, J. A. Martino, P. G. D. Agopian, A. Vandooren, R. Rooyackers, E. Simoen, and C. Claey, “Analysis of current mirror circuits designed with line tunnel FET devices at different temperatures,” Semicond. Sci. Technol., vol. 32, no. 5, pp. 5015-1, 2017.

49. P. G. D. Agopian, J. A. Martino, R. Rooyackers, A. Vandooren, E. Simoen, A. Thean, and C. Claeys, “Intrinsic voltage gain of Line-TFETs and comparison with other TFET and MOSFET architectures,” in Proceedings-Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon, 2016, pp. 13–15.

50. M. D. V. Martino, F. Neves, P. G. D. Agopian, J. A. Martino, A. Vandooren, R. Rooyackers, E. Simoen, A. Thean, and C. Claeys, “Analog performance of vertical nanowire TFETs as a function of temperature and transport mechanism,” Solid. State. Electron., vol. 112, pp. 51–55, 2015.

51. Y. Morita, K. Fukuda, Y. Liu, T. Mori, W. Mizubayashi, Shin-ichi O’uchi, H. Fuketa, S. Otsuka, S. Migita, M. Masahara, K. Endo, H. Ota, and T. Matsukawa, “Tunnel FinFET CMOS inverter with very low short-

circuit current for ultralow-power Internet of Things application," Jpn. J. Appl. Phys., vol. 56, no. 4, 2017.

52. X. Li, M. S. Kim, S. George, A. A. Matthew, J. Nikhil, S. Sampson, S. Gupta, S. Datta, and V. Narayanan, "Emerging Steep-Slope Devices and Circuits: Opportunities and Challenges," in Beyond-CMOS Technologies for Next Generation Computer Design, Cham, Switzerland, Springer, 2019, pp. 195–230.

53. C.-W. Lee, A.N. Nazarov, I. Ferain, N.D. Akhavan, R. Yan, P. Razavi, R. Yu, R.T. Doria, J.-P. Colinge, Low subthreshold slope in junctionless multigate transistors. Appl. Phys. Lett. vol. 96, pp. 102106, 2010.

54. H. Kam, D.T. Lee, R.T. Howe, T.-J. King, A new nano-electro-mechanical field effect transistor (NEMFET) design for low-power electronics, in Tech. Dig. IEEE International Electron Devices Meeting (IEDM), 2005, pp. 463–466.

55. H. Chenming, S. Salahuddin, C.-I. Lin, A. Khan, 0.2 V adiabatic NC-FinFET with 0.6 mA/μm ION and 0.1 nA/μm IOFF, in Proc. Int. Device Research Conference (DRC), 2015, pp. 39–40.

56. S. B. Rahi, S. Tayal, and A. K. Upadhyay, "A review on emerging negative capacitance field effect transistor for low power electronics", Microelectronics Journal, 116, 105242, 2021

57. J. Jo, C. Shin, Negative capacitance field effect transistor with hysteresis-free Sub-60 mV/decade switching. IEEE Electron Device Lett., Vol. 37, no. 3, pp. 245–248, 2016.

58. A. K. Upadhyay, S. B. Rahi, S. Tayal, Y. S. Song, "Recent progress on negative capacitance tunnel FET for low-power applications: Device perspective", Microelectronics Journal, 2022, 105583, ISSN 0026-2692, https://doi.org/10.1016/j.mejo.2022.105583.

59. S. B. Rahi, S. Tayal, J. P. Srivastava, and S. Bhattacharya, "Recent Trends in Compact Modeling of Negative Capacitance Field-Effect Transistors" In Semiconductor Devices and Technologies for Future Ultra Low Power Electronics (pp. 203-226). CRC Press, 2021.

60. Yang Li, Yuye Kang, and Xiao Gong, “Evaluation of Negative Capacitance Ferroelectric MOSFET for Analog Circuit Applications, IEEE Trans. Electron Devices, vol. 64, no. 10, pp. 4317-4321, Oct. 2017.

61. N. Shukla, A. Thathachary, A. Agrawal, H. Paik, A. Aziz, D. Schlom, S. Gupta, R. E. Herbert, S. Datta, A steep-slope transistor based on abrupt electronic phase transition, Nat. Commun. vol. 6, pp. 7812-1–7812-6, 2015.

Note

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9
Investigation of Thermal Performance on Conventional and Junctionless Nanosheet Field Effect Transistors

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Abstract

The analog/RF properties of any device are temperature dependent. Due to a wide range of temperature-sensitive electronic applications including those in the military, nuclear industry, aerospace, telecom, satcoms, IR sensors, and terrestrial industry, the performance of NSFETs at different temperatures must be thoroughly investigated. This chapter briefly analyzes the impact of thermal variations on conventional (CL) and junctionless (JL) Nanosheet Field Effect Transistors (NSFET). The entire investigation has been carried out for temperatures ranging between 100°K-400°K. A thorough investigation of CL NSFET and JL NSFET for different high-k gate dielectrics and spacer dielectrics at a gate length of (L_g)=10nm has been carried out. The analog/RF analysis has been performed at 10µA/µm to focus on the weak/moderate inversion region of operation. When the thermal performance of CL NSFET is compared with the JL NSFET, it is observed that JL NSFET can be chosen for better analog characteristics, whereas CL NSFET is preferred for good RF characteristics of the device. Further, for CL NSFET, a 0.6V Zero Temperature Coefficient (ZTC) point is noticed. This means that the designed CL NSFET exhibits minimal sensitivity to the process and thermal variations. Moreover, for T=100°K, better performance is observed. Also, it is found that high-k gate dielectrics

(k=22) at lower temperatures (100°K) are the best choice in order to optimize the analog/RF device performance for both the CL NSFET and JL NSFET. Furthermore, it is also noticed that spacer dielectrics (K_{SP} =22) at lower temperatures (100°K) are the best choice for analog applications and K_{SP} =8 are the best choice for RF applications.

***Keywords*:** Nanosheet FET, junctionless, thermal effects, analog/RF, high-k, spacer dielectrics

9.1 Introduction

Modern-day CMOS technology is being driven by rising industrial demand for circuitry with high speed, high efficiency, optimized performance, and low power dissipation [1]–[5]. Traditional scaling has dominated semiconductor devices over the past few decades with the goal of an increase in operational speed, lowering power consumption, and increasing transistor density. Threshold voltage roll-off, higher leakage currents, dopant variations, increased power consumption, degradation in subthreshold swing, and design expenses are some of the drawbacks of the traditional Metal Oxide Semiconductor Field Effect Transistor (MOSFET) [6]–[10]. Since the MOSFET acts like a resistor at shorter gate lengths, the drain competes against the gate to take control of the channel. The gate ultimately loses its ability to limit the leakage current pathways that are located at a certain distance from the gate. To address the above issues and mitigate the short channel effects, multi-gate MOSFETs such as Double gate, Tri gate, FinFET, Nanowire FET, and Nanosheet FET are proposed [11]–[15]. However, Double gate, Tri gate, FinFET, and Nanowire FET face short channel effects, poor electrostatics, and worst of all, parasitic capacitances [16]–[21]. Furthermore, the quantity of data that needs to be processed has recently increased tremendously and the need for high-performance (HP) devices has also grown with the arrival of 5G and the big data era. As a result of these technological progressions, Nanosheet FET has been proposed as a next-generation semiconductor device due to excellent short channel effects, higher reliability, and optimized thermal performance [22]–[26]. The formation of sharp junctions is a major challenge to the deep downscaling of FET devices in the nanoscale region [27]–[29]. The idea of junctionless (JL) transistors was proposed by

Colinge *et al.* to solve this issue [30], [31]. Furthermore, recent studies elaborate on a variety of device engineering approaches to improve the functionality of nanoscale devices by reducing SCEs and retaining the electrical characteristics, in line with the prediction made by the international technology roadmap for semiconductors (ITRS). This resulted in a linear improvement in the degree of electronic device integration [32]. Also, the gate oxide layer's thickness (SiO_2) has been reduced to a few nanometers, ensuring the device's functionality. Unfortunately, if the thickness is scaled down below 1 nm, quantum tunneling mechanisms start to take over and power dissipation concerns emerge [33]–[36]. Practically, this challenge can be addressed by adopting a gate oxide made of high dielectric materials (high-*k*) [37], [38]. Nano-devices work best with high-k dielectric materials because their thickness increases with the same capacitance. Both the bandgap and dielectric constant are increased as a result of this. By using high-k materials, the device's gate leakage current can be reduced at a faster pace while consuming less static power. As a result, metal gates combined with high-k dielectrics will likely be employed in modern nano-scaled devices rather than poly-Si gates. Due to their predominance, high-*k* materials are excellent for improving device performance. Furthermore, owing to its excellent thermal stability and relatively high dielectric constant, hafnium dioxide (HfO_2) is considered to have the most potential for high-*k* dielectric materials for applications in nano-scale devices [39]. Furthermore, direct positioning of high-*k* dielectrics atop silicon may cause the performance of FETs to decline due to a weak interface scenario. Researchers proposed gate-stack (GS) technology as a solution to get around this problem. An SiO_2 layer is inserted amidst Silicon and high- *k* dielectric material in this GS technology. Such an integration would help in maintaining the interface quality of Si/SiO_2 and also minimizes the gate tunneling current [40], [41]. Charge sharing is another major problem in nano-scaled devices which occurs due to the close positioning of source, drain, and channel regions. Additionally, the charge sharing causes a rise in the influence of the drain potential on the channel, which leads to SCEs. The gate control is revived by the use of sidewall spacers to combat these effects [42], [43]. However, the addition of sidewall spacers increases the series resistance and messes up the carrier flow, which lowers the on current (I_{ON}) [44]. High-k spacers

are created to address this problem, and they enhance ION through a process known as fringe-induced barrier lowering (FIBL). The fringe electric field provided by high-k spacers reduces the SCEs, as well as the off current (I_{OFF}), and increases the I_{ON} [45], [46]. Modern IC chip design emphasizes thermal-aware design due to increasingly integrated circuit (IC) chip designs. The electrical properties of any device are temperature dependent, and these properties change as the temperature varies [47]–[49]. Due to a wide range of temperature-sensitive electronic applications including those in the military, aerospace, nuclear, transportation, telecom, satcoms, IR sensors, and terrestrial devices, the performance of NSFETs for different temperatures must be thoroughly investigated. Consequently, this chapter aims to provide a deep insight into the thermal performance of conventional and junctionless NSFETs (analog/RF characteristics) with high-k dielectrics and spacer engineering.

9.2 Device Simulation Details

Figure 9.1 shows the 3-dimensional angle of Nanosheet FET (NSFET). Sentaurus TCAD is used for simulating the NSFET device [50]. For conventional (CL) NSFET, the source/drain is doped in the order of 1×10^{20} cm^{-3} and the channel is doped in the order of 1×10^{16} cm^{-3}. For the Junctionless (JL) device, the device is doped uniformly in the order of 1×10^{19} cm^{-3}. Both the devices are n-channel devices. The device specifications of the NSFET are presented in Table 9.1. The gate length (L_g), thickness (T_{SH}), width (W_{SH}), and nanosheet spacing (S_{PSH}) are fixed at 10nm, 5nm, 18nm, and 6nm, respectively. The work functions (ϕ_{ms}) of 4.6eV and 4.8eV are utilized to operate the device in CL and JL mode.

To estimate the gate parasitics, the contact resistivity and silicide resistivity of 7 $\Omega.\mu m^2$ and 7.5Ω/sq. is used, respectively [52]. Temperature has been varied from 100 °K-400 to study the analog/RF performance of CL and JL NSFET. Fermi Dirac statistics, SRH recombination/generation, Auger recombination and Band-to-Band tunneling models, Lombardi Mobility model, and Slotboom Bandgap Narrowing model are used for simulating the device. Moreover, the calibration (I_d-V_g) plot is also shown in Figure 9.2.

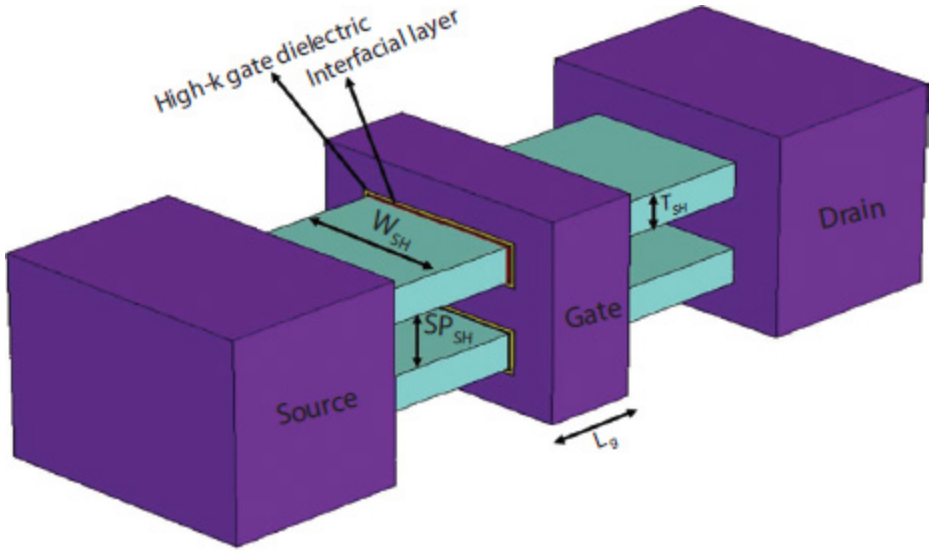

Figure 9.1 3-dimensional view of NSFET.

Table 9.1 Design parameters of NSFET.

Device specifications	**Values**
Gate Length (L_g)	10 nm
Thickness of Sheet (T_{SH})	5 nm
Width of Sheet (W_{SH})	18 nm
Spacing between Sheets (S_{PSH})	6 nm
Work Function (ϕ_{ms})	4.6 eV, 4.8 eV
Contact Resistivity [52]	7 Ω.μm^2
Sheet Silicide Resistivity [52]	7.5 Ω/sq.
Effective Oxide Thickness	0.7 nm
Doping Concentration (Channel) (CL)	1×10^{16} cm^{-3}
Doping Concentration (Source/Drain) (CL)	1×10^{20} cm^{-3}
Doping Concentration (Source/Drain/Channel) (JL)	1×10^{19} cm^{-3}
Temperature	100 °K-400 °K
Gate Dielectric (K)	3.9, 22
Spacer Dielectric (K_{sp})	8, 22

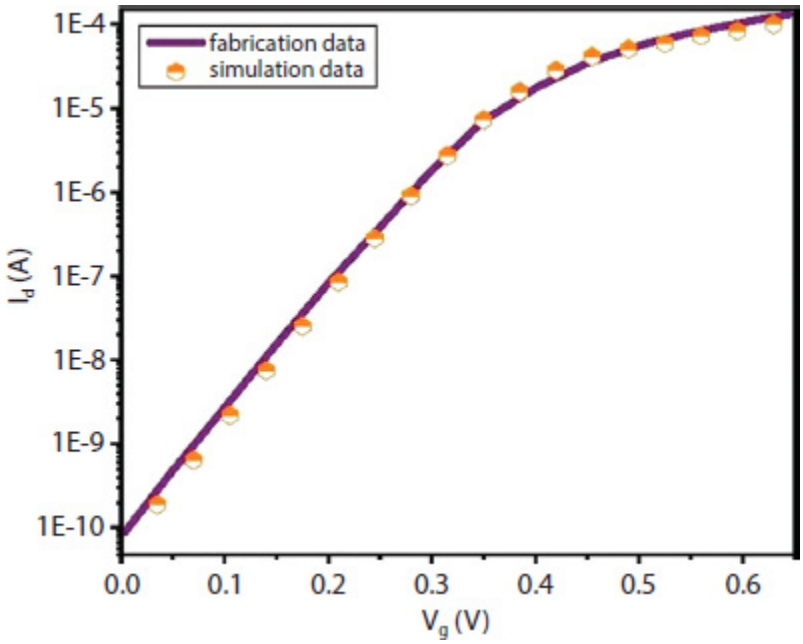

Figure 9.2 Matching of simulated data with experimental data [51].

9.3 Results and Discussion

The circuitry's heavy power consumption and the package's inability to dissipate the heat are what cause the temperature variations. The performance of the device deteriorates as the temperature rises, severely reducing the effectiveness of the VLSI circuit. As a result, it is important to carry out a thorough examination of how temperature affects low power (LP) application zones and to pinpoint strategies for reducing temperature sensitivity. Additionally, it is crucial to look into how FET devices are affected by temperature, particularly in harsh environments where the operating temperature is significantly higher than the standard ambient temperature, for example in the defense and aerospace fields.

9.3.1 Comparison of Thermal Characteristics of Conventional (CL) and Junctionless (JL) NSFET

This subsection briefly discusses the analog/RF performance of conventional and junctionless NSFET at various temperatures ranging from 100-400 K. Figure 9.3 depicts the transfer characteristics of CL and JL NSFET. It can be noticed from Figure 9.3a that at 0.6V we arrive at the Zero Temperature Coefficient (ZTC) point. This means that the designed

CL NSFET exhibits minimal sensitivity to the process and thermal variations. Having been previously studied in silicon device literature, this phenomenon arises from the mutual cancellation of mobility and threshold voltage variations with temperature. After the ZTC point, the drain current (I_d) increases for lower temperatures. The I_d is noticed to be high for 100°K, as shown in Figure 9.3a. On the contrary, it is found that the I_d increases with the increase in temperature. This is because of the increase in mobility of the carriers along the channel area. The relationship for temperature and mobility is given by the below equation:

$$\mu_{eff} = \mu_o \left(\frac{T-2}{T_o} \right)$$

where μ_{eff} = effective mobility

T = lattice temperature

μ_o = mobility at ambient temperature T_o

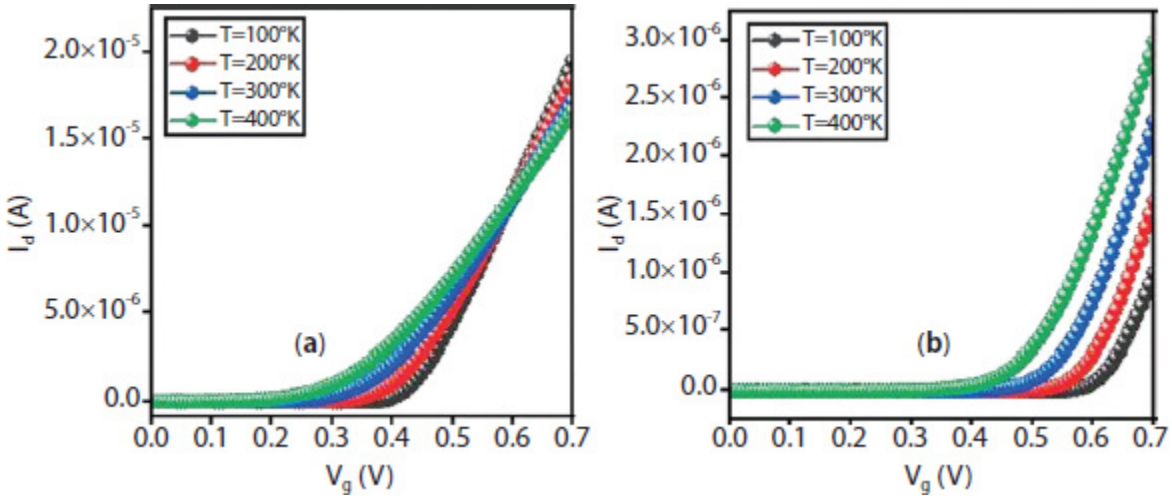

Figure 9.3 I_d-V_g characteristics: (a) CL NSFET; (b) JL NSFET.

Taking a close look at both the graphs, it can be observed that the CL NSFET offers a higher I_d compared to the JL NSFET at all temperatures ranging from 100 °K-400 K.

This can be traced back to the fact that the transconductance efficiency (g_m/I_d) is a key factor that is used in converting dc power to ac frequency

and an increase in g_m/I_d implies an improvement in the device's analog properties. Figure 9.4 shows the g_m/I_d plots of CL NSFET and JL NSFET in conjunction with $I_d/(W/L_g)$ at various temperatures. It is shown that g_m/I_d reduces with an increase in temperature for both CL and JL NSFET. Moreover, it can be seen that JL NSFET shows better gm/Id in comparison to CL NSFET.

The analog/RF characteristics of CL and JL NSFET with respect to temperature are shown in Figure 9.5. The entire analysis is performed for gate length (L_g) =10nm at 10µA/µm to focus the weak/moderate inversion region. The analog/RF characteristics are compared for both the CL NSFET and JL NSFET to find out the suitable device for optimum values. Figure 9.5a shows the transconductance (g_m) and gate to drain conductance (g_{ds}) of the CL NSFET and JL NSFET. Transconductance (g_m) is an important metric for designing operational and transconductance amplifiers. The value of gm denotes an estimation of the drain current's responsiveness to changes in gate-source voltages. In order to determine the intrinsic gain (A_v) of the device, the gate to drain conductance (g_{ds}) is necessary. A low g_{ds} value gives improved analog efficacy. It can be observed that both the g_m and g_{ds} reduce with a rise in temperature for CL NSFET and JL NSFET. Moreover, it is noticed that both the g_m and g_{ds} are high for CL NSFET compared to JL NSFET. This reduction in gm with an increase in temperature might be attributed to lower conduction band energy at higher temperatures. Further, the intrinsic gain (A_v) of the device is given by the following expression:

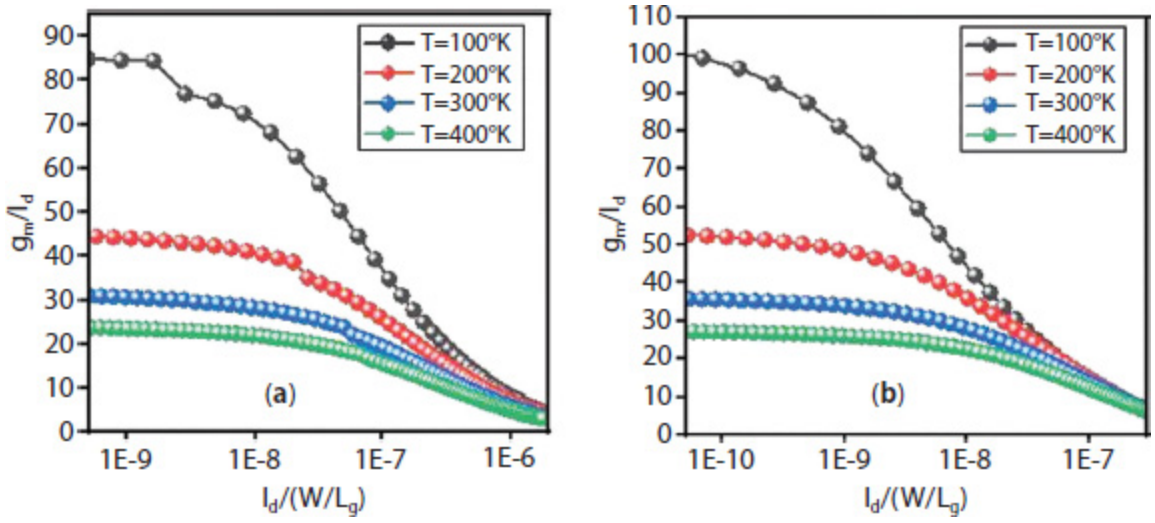

Figure 9.4 g_m/I_d plots: (a) CL NSFET; (b) JL NSFET.

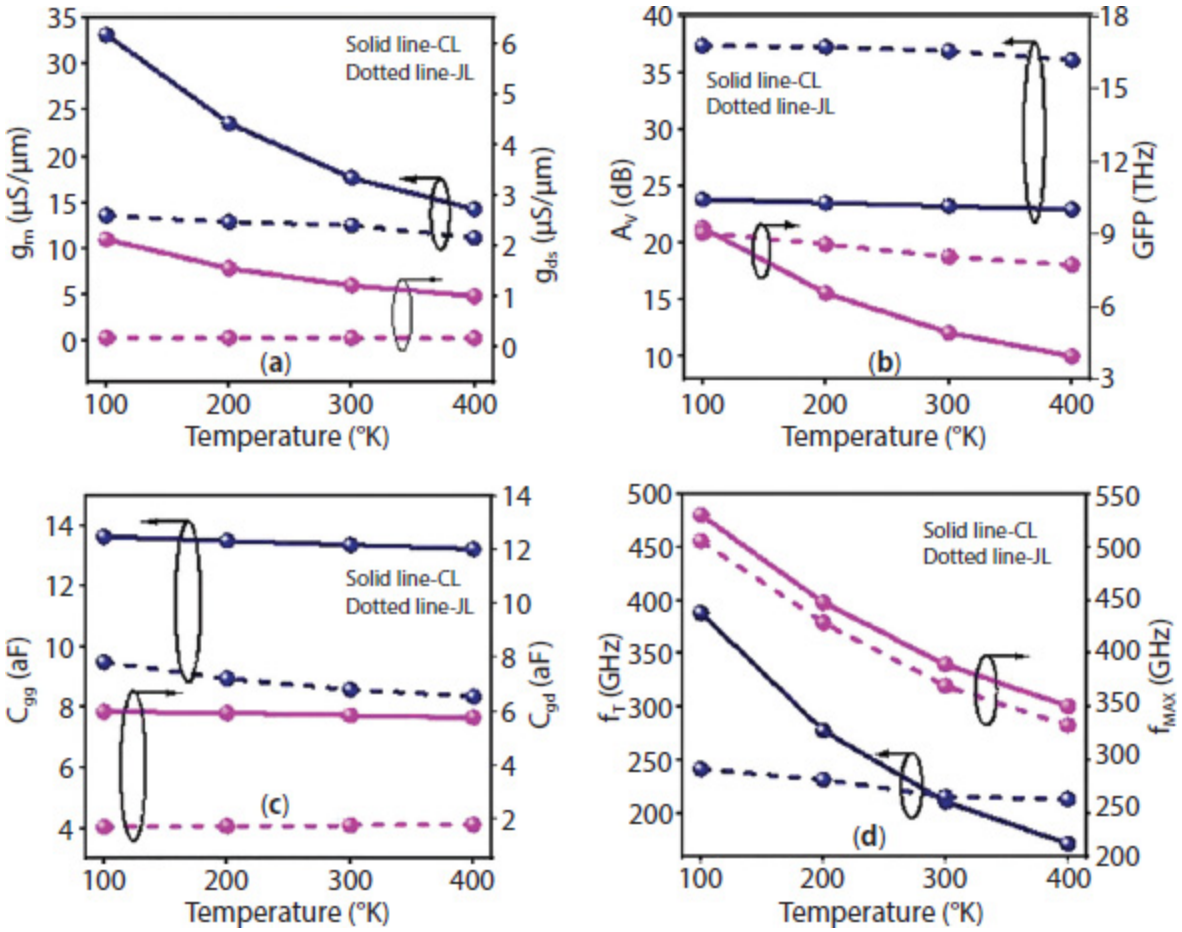

Figure 9.5 Analog/RF parameters of CL and JL NSFET with respect to temperature: (a) g_m, g_{ds}; (b) A_V, GFP; (c) C_{gg}, C_{gd}; (d) f_T, f_{MAX}.

$$A_v = 20log_{10}\left(\frac{g_m}{g_{ds}}\right)$$

From Figure 9.5b, it is observed that A_V of the device decreases for both the CL NSFET and JL NSFET with an increase in temperature. Moreover, A_V is noticed to be high for JL NSFET compared to CL NSFET for all temperatures due to the relative decrement in g_{ds} for JL NSFET in comparison to CL NSFET. Furthermore, gate capacitance (C_{gg}) and gate to drain capacitance (C_{gd}) are the two main metrics that evaluate the RF functionality of the device. For better RF functionality of the device, these capacitances must be kept as low as possible. It is observed that C_{gg} decreases and C_{gd} increases slightly with the increase in temperature for both the CL NSFET and JL NSFET, as shown in Figure 9.5c. When compared to JL NSFET, the CL NSFET showed higher C_{gg} and C_{gd} values at all temperatures. Furthermore, it is also observed from Figure 9.5d that both cutoff frequency $\left(f_T = \frac{g_m}{2\pi C_{gg}}\right)$ and maximum oscillation frequency $\left(f_{MAX} = \frac{f_T}{\sqrt{4R_G(g_{ds} + 2\pi f_T C_{gd})}}\right)$ reduce with the increase in temperature. The reduction in fT at higher temperatures might be due to the relative decrease in gm. The deprivation in gds at higher temperatures might be due to the slight increase in Cgd at higher temperatures. Furthermore, CL NSFET has recorded better f_T and f_{MAX} values compared to JL NSFET, as seen in Figure 9.5d. Additionally, when constructing op-amps for high-frequency (HF) applications, the Gain Frequency Product (GFP = ($A_V \times f_T$) is a crucial consideration. It is shown that GFP decreases with an increase in temperatures for CL NSFET and JL NSFET. This might be due to the relative decrement in both the A_V and f_T with respect to increases in temperatures for both devices. Furthermore, JLNSFET has obtained better GFP in comparison to CL NSFET due to the relative improvement in gds values compared to gm and f_T. Consequently, it is suggested that JL NSFET is preferred for better analog performance and CL NSFET is preferred for good RF performance of the device.

9.3.2 Comparison of Thermal Performance of High-k Gate Dielectrics for CL NSFET and JL NSFET

As discussed in Section 9.1, high-k gate dielectrics play a very important role in optimizing device performance. This subsection discusses the impact of temperature on high-k gate dielectrics for both CL NSFET and JL NSFET. Hafnium dioxide (HfO_2) having a dielectric constant of k=22 is employed as a high-k gate dielectric and its performance is compared with the low-k gate dielectric SiO_2, with dielectric constant k=3.9, to find the suitable gate dielectric for CL NSFET as well as JL NSFET. Figure 9.6 shows the Id-Vg plots for CL NSFET as well as JL NSFET. It is shown that the use of high-k dielectric material (k=22) degrades the Id for both devices. Similar to k=3.9, k =22 also experienced a ZTC point at Vgs=0.6V. Later on, the lower temperatures recorded higher Id values for CL NSFET. The gm/Id in conjunction with Id/(W/Lg) for different dielectric constants for several temperatures is shown in Figure 9.7. It is shown that the utilization of k=22 yielded higher gm/Id values for both the CL NSFET and JL NSFET for all temperatures. Moreover, it is observed that lower temperatures yielded better gm/Id values for both devices. However, a better improvement in gm/Id is obtained with JL NSFET compared to the CL NSFET.

The analog/RF characteristics of k=3.9 and k=22 for various temperatures are shown in Figure 9.8. It is shown that gm and gds are improved greatly for k=22 compared to k=3.9 at all temperatures for both devices. The g_m and g_{ds} are found to be decreasing with an increase in temperature for CL NSFET and JL NSFET. Moreover, it should be noted that CL NSFET showed superior performance compared to JL NSFET in terms of g_m for both the dielectrics, whereas JL NSFET recorded excellent performance in comparison to CL NSFET in terms of g_{ds} reduction.

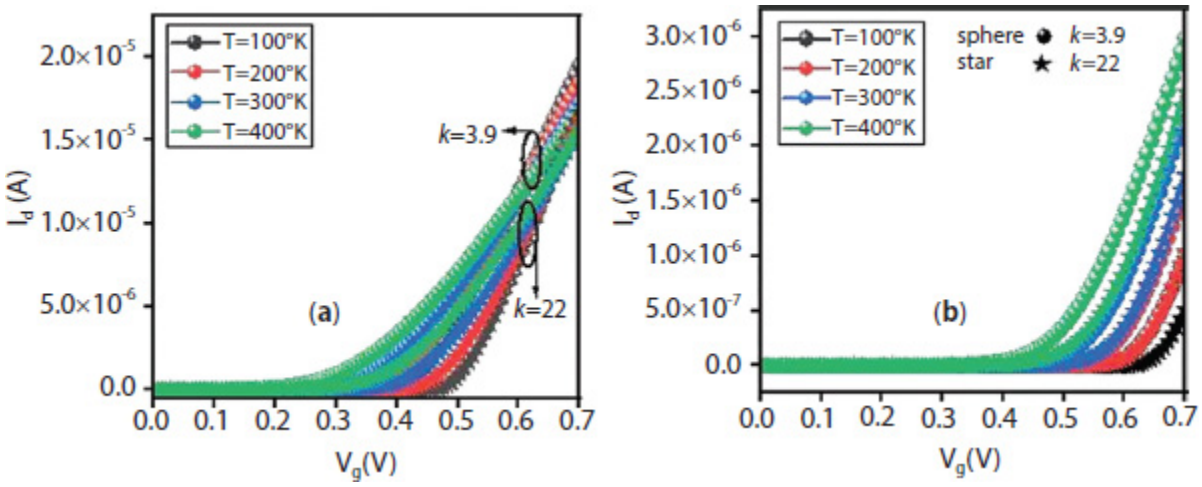

Figure 9.6 Id-Vg characteristics of different dielectrics at various temperatures: (a) CL NSFET; (b) JL NSFET.

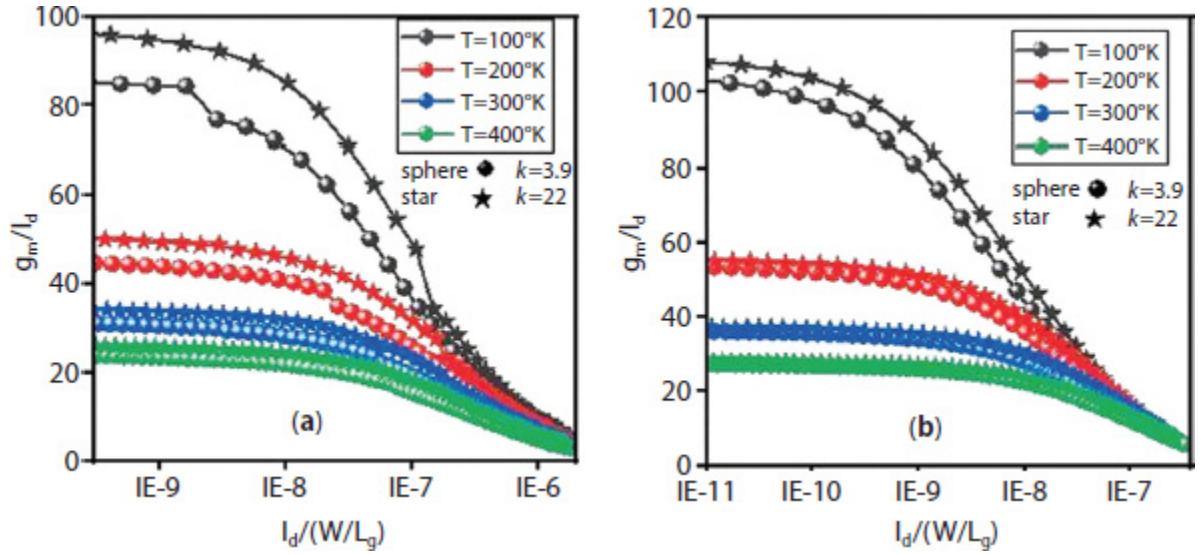

Figure 9.7 gm/Id plots of different dielectrics at various temperatures: (a) CL NSFET; (b) JL NSFET.

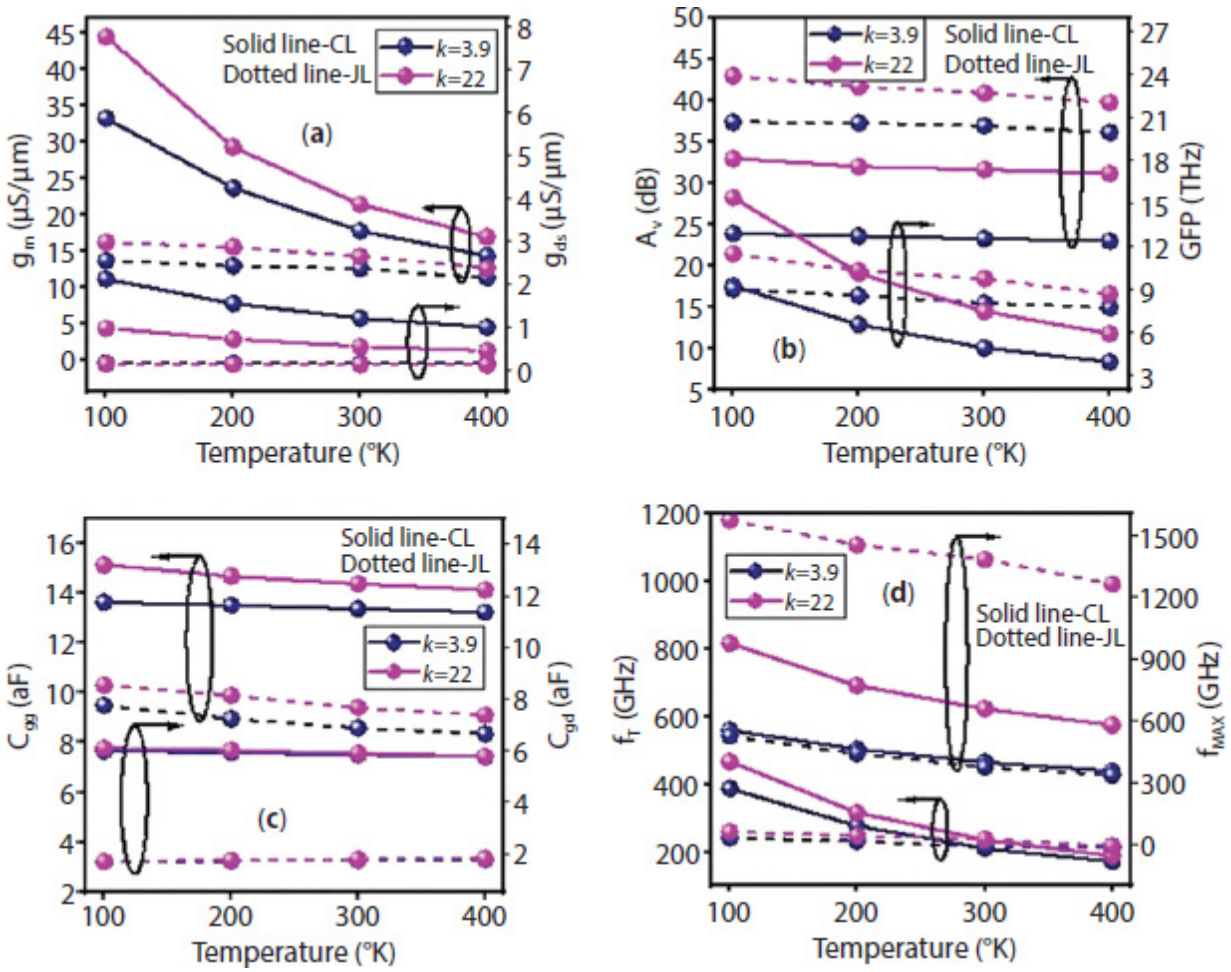

Figure 9.8 Analog/RF parameters of CL and JL NSFET with respect to temperature for different dielectric constants: (a) g_m, g_{ds}; (b) A_V, GFP; (c) C_{gg}, C_{gd}; (d) f_T, f_{MAX}.

This relative decrement in gds for JL NSFET further improved the AV for *k*=22, as depicted in Figure 9.8b. The utilization of *k*=22 rather than *k*=3.9 for both the CL NSFET and JL NSFET gave better gain. Furthermore, it is observed that Cgg is increasing for *k*=22 in comparison to *k*=3.9 for both devices. However, Cgd is almost the same for both devices at *k* =3.9 and *k* =22, as shown in Figure 9.8c. Moreover, it is also noticed that CL NSFET exhibited higher capacitance values compared to the JL NSFET. Although Cgg is higher for *k*=22, the relative improvement in gm is greater compared to the increase in Cgg and the fT is higher for *k*=22 in comparison to *k* =3.9, as picturized in Figure 9.8d. As the Cgd and gds values are found to be low for *k* =22, the fMAX is observed to be high for *k* =22 compared to *k* =3.9. Moreover, it is also noticed that GFP is higher for *k* =22 in comparison to *k*

=3.9. Consequently, it can be seen that high-*k* gate dielectrics (*k* =22) at lower temperatures (100°K) are the best choice in order to optimize the device performance for both the CL NSFET and JL NSFET.

9.3.3 Comparison of Thermal Performance of Spacer Dielectrics for CL NSFET and JL NSFET

This subsection discusses the impact of temperature (100-400 °K) on spacer dielectrics for both the CL NSFET and JL NSFET. Silicon Nitride ($S_{i3}N_4$) and Hafnium dioxide (HfO_2) having dielectric constants of K_{SP} =8 and K_{SP} =22, respectively, are employed as spacer dielectrics to find the suitable spacer dielectric for CL NSFET as well as JL NSFET.

Figure 9.9 shows the I_d-V_g plots for CL NSFET as well as JL NSFET. It is shown that the use of high- *k* spacer material (K_{SP}=22) degrades the Id for both devices. The CL NSFET for both the spacer dielectrics experienced a ZTC point at V_{gs}=0.6V. Later, the lower temperatures recorded higher Id values for CL NSFET. The g_m/I_d in conjunction with $I_d/(W/L_g)$ for different dielectric constants for several temperatures is shown in Figure 9.10. It is shown that the utilization of K_{SP}=22 produced higher g_m/I_d values for both the CL NSFET and JL NSFET at all temperatures compared to K_{SP}=8. This indicates better input drivability for HfO_2 spacers.

Moreover, it is observed that lower temperatures yielded better g_m/I_d values for both devices. However, an improvement in gm/Id is obtained with JL NSFET compared to CL NSFET.

The analog/RF characteristics of K_{SP}=8 and K_{SP}=22 for various temperatures are portrayed in Figure 9.11. It can is shown that g_m and g_{ds} are improved greatly for K_{SP}=22 compared to K_{SP}=8 at all temperatures for both devices (Figure 9.11a). The g_m and g_{ds} are found to be decreasing with the increase in temperature for CL NSFET and JL NSFET. Moreover, it can be noticed that CL NSFET showed superior performance compared to JL NSFET in terms of gm for both the spacer dielectrics, whereas JL NSFET recorded excellent performance in comparison with CL NSFET in terms of g_{ds} reduction. This reduction of g_{ds} indicates channel control through the

drain is reduced with HfO_2 as the spacer dielectric that in turn reduces the impact of channel length modulation (CLM), making the device suitable for constant current source applications. This relative decrement in g_{ds} for JL NSFET further improved the A_V for K_{SP}=22, as shown in Figure 9.11b. The utilization of K_{SP}=22 instead of K_{SP}=8 for both CL NSFET and JL NSFET gave better gain. Furthermore, it is observed that Cgg and Cgd are decreasing for K_{SP}=22 and K_{SP}=8 for both devices (Figure 9.11c). As K_{SP} increases, the fringing field component of the device increases and hence C_{gg} and C_{gd} increase, as shown in Figure 9.11c, and is less when employed with Si_3N_4. Moreover, it is also shown that CL NSFET exhibited higher capacitance values compared to the JL NSFET. Since C_{gg} is higher for K_{SP} =22, the f_T is lower for K_{SP}=22 in comparison to K_{SP}=8, as picturized in Figure 9.11d. Since the C_{gd} values are low for K_{SP}=8, the f_{MAX} is observed to be high for K_{SP}=8 compared to K_{SP}=8. Moreover, it is also shown that GFP is higher for K_{SP}=8 in comparison to K_{SP}=22 for JL NSFET and lower for K_{SP}=8 for CL NSFET. Consequently, it can be seen that spacer dielectrics (K_{SP}=22) at lower temperatures (100°K) are the best choice for analog applications and K_{SP}=8 are the best choice for RF applications.

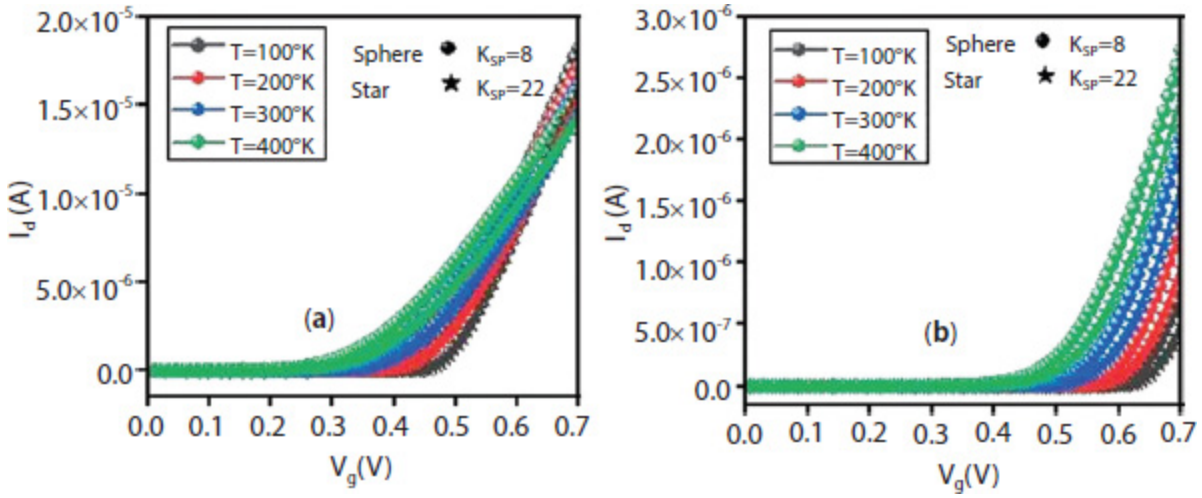

Figure 9.9 I_d-V_g characteristics of different spacer dielectrics at various temperatures: (a) CL NSFET; (b) JL NSFET.

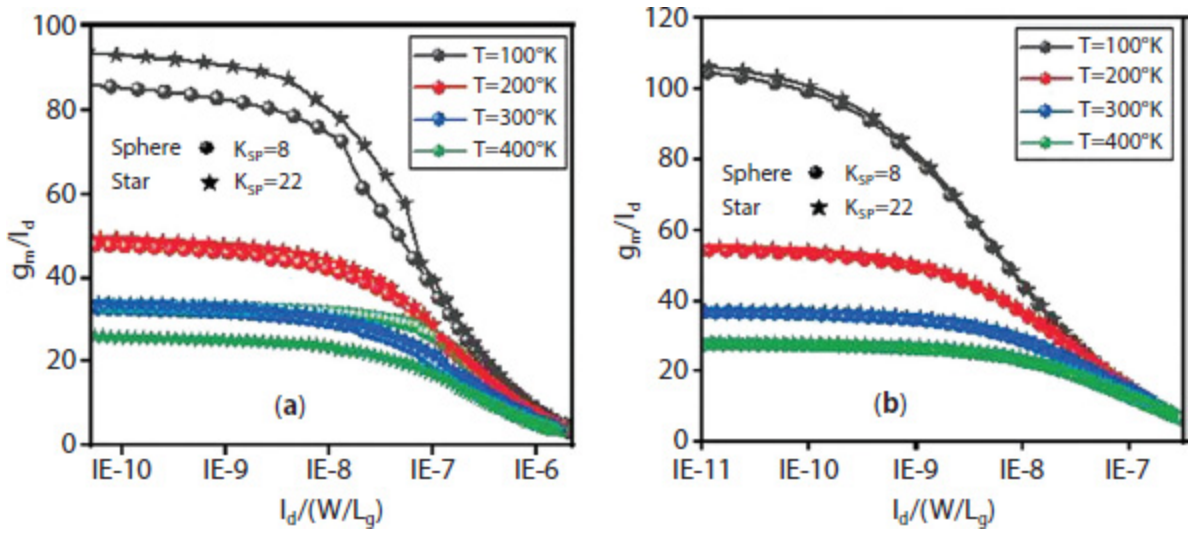

Figure 9.10 gm/Id plots of different spacer dielectrics at various temperatures: (a) CL NSFET; (b) JL NSFET.

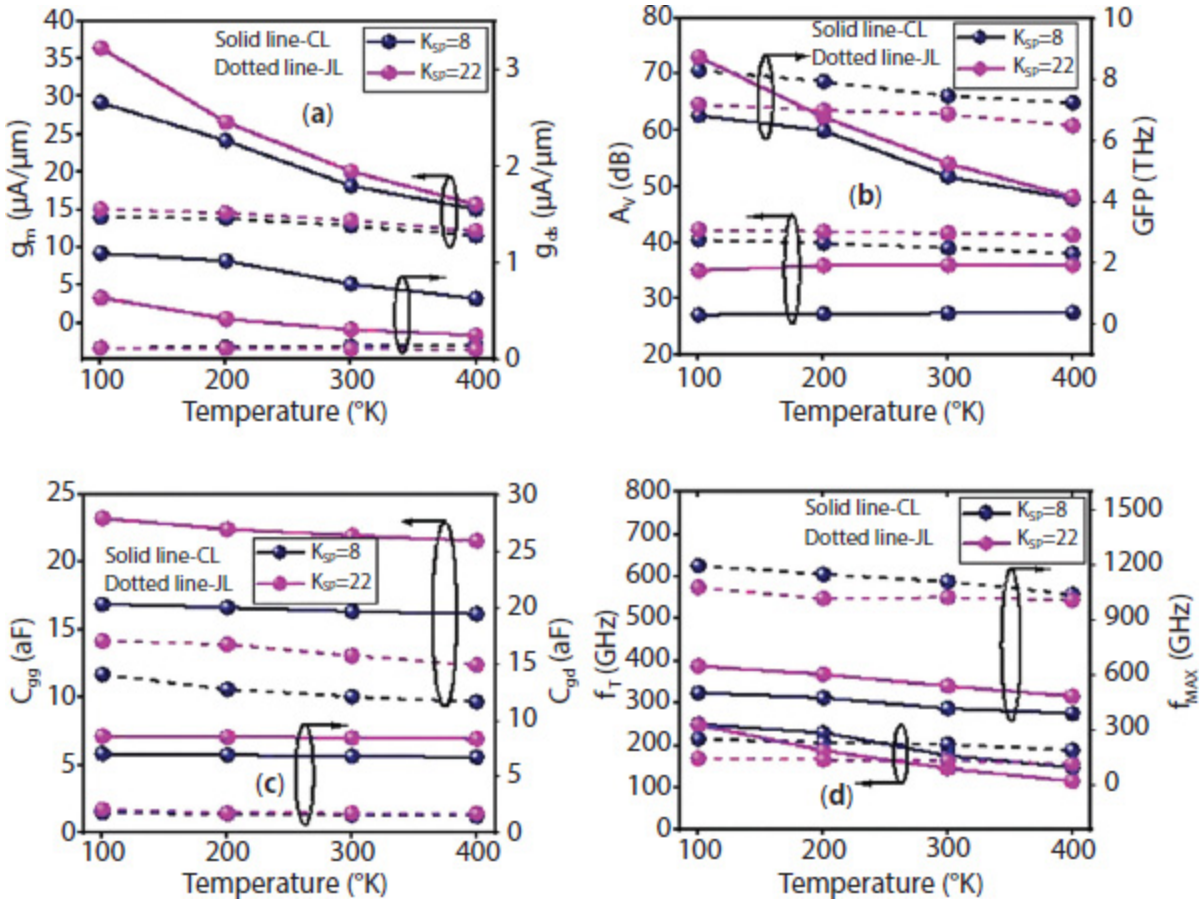

Figure 9.11 Analog/RF parameters of CL and JL NSFET in conjunction with temperature for different spacer dielectric constants: (a) gm, gds; (b) AV, GFP; (c) Cgg, Cgd; (d) fT, fMAX.

9.4 Conclusion

This paper briefly addressed the thermal effects of CL NSFET and JL NSFET with L_g, T_{SH}, and W_{SH} equaling 10nm, 5nm, and 18nm, respectively. The analog/RF analysis has been performed for temperatures ranging between 100°K-400°K for high-*k* dielectrics and spacer dielectrics. The comparison of analog/RF performance for CL NSFET and JL NSFET has been carried out and it has been observed that g_m and g_{ds} decrease with an increase in temperature for CL NSFET and JL NSFET. Also, A_V is high for JL NSFET compared to CL NSFET for all temperatures due to the relative decrement in g_{ds} for JL NSFET in comparison with CL NSFET. When compared to JL NSFET, the CL NSFET showed higher C_{gg} and C_{gd} values at all temperatures. Furthermore, CL NSFET has recorded the best f_T and f_{MAX} values compared to JL NSFET. Moreso, JL NSFET has obtained better GFP in comparison with CL NSFET. Hence, it is suggested that JL NSFET is preferred for better analog performance and CL NSFET is preferred for good RF performance of the device for better thermal performance. Further, for high-*k* gate dielectrics, it is noticed that CL NSFET showed superior performance compared to JL NSFET in terms of gm for both the dielectrics, whereas JL NSFET recorded excellent performance in comparison with CL NSFET in terms of g_{ds} reduction. The utilization of *k*=22 instead of *k*=3.9 for both the CL NSFET and JL NSFET gave better gain. It is also found that GFP is higher for *k*=22 in comparison to =3.9. Overall, high-*k* gate dielectrics (*k* =22) at lower temperatures (100°K) are the best choice to optimize device performance for both the CL NSFET and JL NSFET. Furthermore, for spacer dielectrics, it is observed that gm and gds are improved greatly for K_{SP}=22 compared to K_{SP}=8 at all temperatures for both devices. Moreover, the utilization of K_{SP}=22 instead of K_{SP}=8 for both the CL NSFET and JL NSFET gave better gain. Also, as the K_{SP} increases, the fringing field component of the device increased and hence C_{gg} and C_{gd} increased. This is less when employed with Si_3N_4. Consequently, spacer dielectrics (K_{SP}=22) at lower temperatures (100°K) are the best choice for analog applications and K_{SP}=8 are the best choice for RF applications.

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References

[1] M. Figueiredo, R. Santos-Tavares, E. Santin, J. Ferreira, G. Evans, and J. Goes, “A two- stage fully differential inverter-based self-biased CMOS amplifier with high efficiency,” IEEE Trans. Circuits Syst. I Regul. Pap., vol. 58, no. 7, pp. 1591–1603, 2011, doi: 10.1109/TCSI.2011.2150910.

[2] L. Chang, M. Ieong, and M. Yang, “CMOS Circuit Performance Enhancement by Surface Orientation Optimization,” Simul. Semicond. Process. Devices 2004, pp. 57–60, 2004, doi: 10.1007/978-3-7091-0624-2_14.

[3] R. X. Gu and M. I. Elmasry, “Power dissipation analysis and optimization of deep submicron CMOS digital circuits,” IEEE J. Solid-State Circuits, vol. 31, no. 5, pp. 707– 713, 1996, doi: 10.1109/4.509853.

[4] R. H. Krambeck, C. M. Lee, and H. F. S. Law, “High-Speed Compact Circuits with CMOS,” IEEE J. Solid-State Circuits, vol. 17, no. 3, pp. 614–619, 1982, doi: 10.1109/JSSC.1982.1051786.

[5] S. Valasa, J. R. Shinde, D. R. Ramji, and S. Avunoori, “A Power and Delay Efficient Circuit for CMOS Phase Detector and Phase Frequency Detector,” Proc. 6th Int. Conf. Commun. Electron. Syst. ICCES 2021, pp. 77–82, 2021, doi: 10.1109/ICCES51350.2021.9489140.

[6] G. Ghibaudo, M. Aouad, M. Casse, S. Martinie, T. Poiroux, and F. Balestra, “On the modelling of temperature dependence of subthreshold swing in MOSFETs down to cryogenic temperature,” Solid. State. Electron., vol. 170, 2020, doi: 10.1016/j.sse.2020.107820.

[7] A. Mihaila, F. Udrea, G. Amaratunga, and G. Brezeanu, “A comprehensive analysis of breakdown mechanisms in 4H-SiC MOSFET

and JFET," Proc. Int. Semicond. Conf. CAS, vol. 1, pp. 185–188, 2000, doi: 10.1109/ smicnd.2000.890214.

[8] T. Endoh and Y. Norifusa, "Scalability of vertical MOSFETs in sub-10nm generation and its mechanism," IEICE Trans. Electron., vol. E92-C, no. 5, pp. 594–597, 2009, doi: 10.1587/transele.E92.C.594.

[9] M. Nishisaka, S. Matsumoto, and T. Asano, "Schottky source/drain SOI MOSFET with shallow doped extension," Japanese J. Appl. Physics, Part 1 Regul. Pap. Short Notes Rev. Pap., vol. 42, no. 4 B, pp. 2009–2013, 2003, doi: 10.1143/jjap.42.2009.

[10] Y. Omura, A. Mallik, and N. Matsuo, "The Potential and the Drawbacks of Underlap Single-Gate Ultrathin SOI MOSFET," MOS Devices Low-Voltage Low-Energy Appl., pp. 180–193, 2016, doi: 10.1002/9781119107361.ch17.

[11] N. Guduri, "Performance Analysis of Dielectrically Separated Independent Gates Junctionless DG-MOSFET : A Digital Perspective," pp. 9–12.

[12] S. Katharashala, "Impact of Channel Thickness on the Performance of JL-DG MOSFET based NAND , NOR , and NOT Logic Gates," pp. 8–11.

[13] S. Tayal and A. Nandi, "Comparative analysis of High-K gate stack based Conventional Junctionless FinFET," 2017 14th IEEE India Counc. Int. Conf. INDICON 2017, 2018, doi: 10.1109/INDICON.2017.8487675.

[14] V. B. Sreenivasulu and V. Narendar, "Junctionless Gate-all-around Nanowire FET with Asymmetric Spacer for Continued Scaling," Silicon, 2021, doi: 10.1007/s12633-021-01471-z.

[15] B. S. Vakkalakula and N. Vadthiya, "p-Type Trigate Junctionless Nanosheet MOSFET: Analog/RF, Linearity, and Circuit Analysis," ECS J. Solid State Sci. Technol., vol. 10, no. 12, p. 123001, 2021, doi: 10.1149/2162-8777/ac3bdf.

[16] J. J. Kim and K. Roy, “Double gate-MOSFET subthreshold circuit for ultralow power applications,” IEEE Trans. Electron Devices, vol. 51, no. 9, pp. 1468– 1474, 2004, doi: 10.1109/TED.2004.833965.

[17] R. S. Pal, S. Sharma, and S. Dasgupta, “Recent trend of FinFET devices and its challenges: A review,” 2017 Conf. Emerg. Devices Smart Syst. ICEDSS 2017, pp. 150–154, 2017, doi: 10.1109/ICEDSS.2017.8073675.

[18] S. S. Rodriguez, J. C. Tinoco, A. G. Martinez-Lopez, J. Alvarado, and J. P. Raskin, “Parasitic gate capacitance model for triple-gate finfets,” IEEE Trans. Electron Devices, vol. 60, no. 11, pp. 3710–3717, 2013, doi: 10.1109/ TED.2013.2282629.

[19] K. W. Lee, T. Y. An, S. Y. Joo, K. W. Kwon, and S. Y. Kim, “Modeling of parasitic fringing capacitance in multifin trigate FinFETs,” IEEE Trans. Electron Devices, vol. 60, no. 5, pp. 1786–1789, 2013, doi: 10.1109/TED.2013.2252467.

[20] S. Barraud *et al.*, “Opportunities and challenges of nanowire-based CMOS technologies,” 2015 IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. S3S 2015, 2015, doi: 10.1109/S3S.2015.7333520.

[21] J. Zhuge, R. Wang, R. Huang, X. Zhang, and Y. Wang, “Investigation of parasitic effects and design optimization in silicon nanowire MOSFETs for RF applications,” IEEE Trans. Electron Devices, vol. 55, no. 8, pp. 2142–2147, 2008, doi: 10.1109/TED.2008.926279.

[22] D. Yakimets *et al.*, “Power aware FinFET and lateral nanosheet FET targeting for 3nm CMOS technology,” Tech. Dig. - Int. Electron Devices Meet. IEDM, pp. 20.4.1-20.4.4, 2018, doi: 10.1109/IEDM.2017.8268429.

[23] S. Valasa, S. Tayal, and L. R. Thoutam, “Design Insights into Thermal Performance of Vertically Stacked JL-NSFET with High-k Gate Dielectric for Sub 5-nm Technology Node,” ECS J. Solid State Sci. Technol., vol. 11, no. 4, p. 041008, 2022, doi: 10.1149/2162-8777/ac6627.

[24] D. Nagy, G. Espineira, G. Indalecio, A. J. Garcia-Loureiro, K. Kalna, and N. Seoane, “Benchmarking of FinFET, Nanosheet, and Nanowire FET Architectures for Future Technology Nodes,” IEEE Access, vol. 8, pp. 53196– 53202, 2020, doi: 10.1109/ACCESS.2020.2980925.

[25] M. K. N., “Energy and Power Efficient System on Chip With Nanosheet Fet,” J. Electron. Informatics, vol. 01, no. 01, pp. 51–59, 2019, doi: 10.36548/ jei.2019.1.006.

[26] S. Valasa, S. Tayal, and L. R. Thoutam, “Optimization of Design Space for Vertically Stacked Junctionless Nanosheet FET for Analog/RF Applications,” Silicon, 2022, doi: 10.1007/s12633-022-01793-6.

[27] N. Trivedi, M. Kumar, S. Haldar, S. S. Deswal, M. Gupta, and R. S. Gupta, “Analytical modeling of Junctionless Accumulation Mode Cylindrical Surrounding Gate MOSFET (JAM-CSG),” Int. J. Numer. Model. Electron. Networks, Devices Fields, vol. 29, no. 6, pp. 1036–1043, 2016, doi: 10.1002/ jnm.2162.

[28] N. A. Kumari and P. Prithvi, “Performance Evaluation of GAA Nanosheet FET with Varied Geometrical and Process Parameters,” Silicon, 2022, doi: 10.1007/s12633-022-01695-7.

[29] T. Solankia and N. Parmar, “A Review paper : A Comprehensive study of Junctionless transistor,” Natl. Conf. Recent Trends Eng. Technol., pp. 1–5, 2011.

[30] J. P. Colinge *et al.*, “Junctionless Transistors: Physics and Properties,” Eng. Mater., pp. 187– 200, 2011, doi: 10.1007/978-3-642-15868-1_10.

[31] A. Kranti *et al.*, “Junctionless nanowire transistor (JNT): Properties and design guidelines,” 2010 Proc. Eur. Solid State Device Res. Conf. ESSDERC 2010, pp. 357–360, 2010, doi: 10.1109/ESSDERC.2010.5618216.

[32] “https://en.wikipedia.org/wiki/International_Technology_Roadmap_for_Semiconductors.”

[33] A. Ohata, “Evaluation of performance degradation factors for high-k gate dielectrics in N- channel MOSFETs,” Solid. State. Electron., vol. 48, no. 2, pp. 345–349, 2004, doi: 10.1016/S0038-1101(03)00294-6.

[34] S. Tayal and A. Nandi, “ Effect of High- K Gate Dielectric In-Conjunction with Channel Parameters on the Performance of FinFET Based 6T SRAM ,” J. Nanoelectron. Optoelectron., vol. 13, no. 5, pp. 768–774, 2018, doi: 10.1166/ jno.2018.2287.

[35] G. Ribes *et al.*, “Review on high-k dielectrics reliability issues,” IEEE Trans. Device Mater. Reliab., vol. 5, no. 1, pp. 5–19, 2005, doi: 10.1109/ TDMR.2005.845236.

[36] S. K. . Mohapatra, K. P. Pradhan, and P. K. Sahu, “Influence of High-k Gate Dielectric on Nanoscale DG-MOSFET,” Int. J. Adv. Sci. Technol., vol. 65, pp. 19–26, 2014, doi: 10.14257/ijast.2014.65.02.

[37] S. Tayal and A. Nandi, “Interfacial layer dependence of High-K gate stack based Conventional trigate FinFET concerning analog/RF performance,” Proc. 4th Int. Conf. Devices, Circuits Syst. ICDCS 2018, pp. 305–308, 2019, doi: 10.1109/ICDCSyst.2018.8605172.

[38] J. P. Locquet, C. Marchiori, M. Sousa, J. Fompeyrine, and J. W. Seo, “High-K dielectrics for the gate stack,” J. Appl. Phys., vol. 100, no. 5, 2006, doi: 10.1063/1.2336996.

[39] R. C. Smith *et al.*, “Chemical vapour deposition of the oxides of titanium, zirconium and hafnium for use as high-k materials in microelectronic devices. A carbon-free precursor for the synthesis of hafnium dioxide,” Adv. Mater. Opt. Electron., vol. 10, no. 35, pp. 105–114, 2000, doi: 10.1002/1099-0712(200005/10)10:3/5<105::aid-amo402>3.3.co;2-a.

[40] X. Klemenschits, S. Selberherr, and L. Filipovic, “Modeling of gate stack patterning for advanced technology nodes: A review,” Micromachines, vol. 9, no. 12, 2018, doi: 10.3390/mi9120631.

[41] S. K. Das, U. Nanda, S. M. Biswal, C. K. Pandey, and L. I. Giri, “Performance Analysis of Gate-Stack Dual-Material DG MOSFET Using Work-Function Modulation Technique for Lower Technology

Nodes," Silicon, vol. 14, no. 6, pp. 2965–2973, 2022, doi: 10.1007/s12633-021-01095-3.

[42] S. Gupta and A. Nandi, "Effect of air spacer on analog performance of underlap tri-gate FinFET," Superlattices Microstruct., vol. 109, pp. 693–701, 2017, doi: 10.1016/j.spmi.2017.05.053.

[43] D. Ryu, I. Myeong, J. K. Lee, M. Kang, J. Jeon, and H. Shin, "Investigation of gate sidewall spacer optimization from OFF-state leakage current perspective in 3-nm node device," IEEE Trans. Electron Devices, vol. 66, no. 6, pp. 2532–2537, 2019, doi: 10.1109/TED.2019.2912394.

[44] D. Ryu, M. Kim, J. Yu, S. Kim, J. H. Lee, and B. G. Park, "Investigation of Sidewall High- k Interfacial Layer Effect in Gate-All-Around Structure," IEEE Trans. Electron Devices, vol. 67, no. 4, pp. 1859–1863, 2020, doi: 10.1109/TED.2020.2975255.

[45] S. Tayal and A. Nandi, "Effect of FIBL in-conjunction with channel parameters on analog and RF FOM of FinFET," Superlattices Microstruct., vol. 105, pp. 152–162, 2017, doi: 10.1016/j.spmi.2017.03.018.

[46] F. Ma, H. X. Liu, Q. W. Kuang, and J. Bin Fan, "The influence and explanation of fringing- induced barrier lowering on sub-100 nm MOSFETs with high-k gate dielectrics," Chinese Phys. B, vol. 21, no. 5, 2012, doi: 10.1088/1674-1056/21/5/057305.

[47] J. H. Choi, J. Murthy, and K. Roy, "The effect of process variation on device temperature in FinFET circuits," IEEE/ACM Int. Conf. Comput. Des. Dig. Tech. Pap. ICCAD, pp. 747– 751, 2007, doi: 10.1109/ICCAD.2007.4397355.

[48] S. Tayal *et al.*, "Investigation of Nanosheet-FET Based Logic Gates at Sub-7 nm Technology Node for Digital IC Applications," Silicon, 2022, doi: 10.1007/ s12633-022-01934-x.

[49] S. Tayal, V. Mittal, S. Jadav, S. Gupta, A. Nandi, and B. Krishan, "Temperature sensitivity analysis of inner-gate engineered JL-SiNT-

FET: An Analog/ RF prospective," Cryogenics (Guildf)., vol. 108, 2020, doi: 10.1016/j. cryogenics.2020.103087.

[50] "https://www.synopsys.com/silicon/tcad/process-simulation/sentaurus-process.html."

[51] N. Loubet *et al.*, "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," Dig. Tech. Pap. - Symp. VLSI Technol., pp. T230–T231, 2017, doi: 10.23919/VLSIT.2017.7998183.

[52] S. Nuttinck, B. Parvais, G. Curatola, and A. Mercha, "Double-gate finFETs as a CMOS technology downscaling option: An RF perspective," IEEE Trans. Electron Devices, vol. 54, no. 2, pp. 279–283, 2007, doi: 10.1109/ TED.2006.888670.

Note

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10
Introduction to Newly Adopted NCFET and Ferroelectrics for Low-Power Application

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Abstract

In the 21st century, the lifestyle of every individual is dependent on various electronic gadgets such as laptops, cameras, mobiles, smart watches, etc. All devices directly or indirectly rely on transistors. The demand for an increase in speed, processing capability, memory, and applications of these electronic appliances lead to aggressive scaling of MOS devices/transistors. Numerous challenges such as power management, fabrication complexity, and voltage scaling have been encountered with CMOS scaling. The reliable solution to these challenges is to overcome the thermionic limit of a subthreshold slope (SS) of 60 mV/Dec in transistors. Negative Capacitance FETs (NCFETs) are one of the most efficient methods to achieve SS below 60 mV/Dec with no extensive amendments in existing processes for CMOS fabrication. In NCFETs, the accumulation of just a thin layer of ferroelectric over the gate-stack can provide a desired SS, i.e., below 60 mV/Dec, because of internal voltage amplification that does not degrade any on-state characteristics. Since the last decade, the concept of NC has been accommodated with various device structures. It is noticed that NCFET not only results in steep SS and low power, but it also miniaturizes various Short Channel Effects (SCEs) such as Negative Drain induced Barrier Lowering (DIBL), low leakage current, Negative Differential Resistance (NDR), etc., and that makes it an excellent candidature for future low power applications. Still, there are some challenges in NCFETs related to their design for minimal energy consumption, ferroelectric material and its thickness, hysteresis, structure, stability, and capacitance matching. The NCFETs also face high Gate Induced Drain Leakage (GIDL) Current. Thus,

this chapter includes the various aspects related to performance and design of NCFETs for low-power applications, as well as the critical issue of high GIDL current.

***Keywords*:** Negative capacitance, ferroelectric, low power, NCFET, Steep SS, negative DIBL

10.1 Introduction

Nowadays, chip manufacturers are presenting endless efforts to fabricate a greater number of transistors on a single chip in reaction to the demand in today's market and pioneering applications. The relentless down-scaling of MOSFET is happening to achieve a chip with the fastest response, higher packaging density, new wireless systems, etc. This led to the end of Dennard's scaling in the 21st century's semiconductor industry [1]. According to Dennard's Scaling Rule, the voltage at which transistors operate will also reduce with the size of the transistor to maintain the perpetual electric field. But, a huge number of billions to trillions of transistors with non-scalable operating voltage on a single chip led to excessive heat, and thermal and power mismanagement [2, 3]. This ever-rising heat and power became the major bottleneck for further technology scaling and restricted the capability of existing cooling techniques [4-6]. Moreover, as per the aviation report, this excessive heat also led to an increase in global CO_2 emissions and rise in global warming [7, 8]. Thus, the main concern of the semiconductor industry is to attain a proper control over thermal and power management with the downscaling. Along with this, it is also important to overcome various other challenges related to scaling such as short channel effects (SCEs) that arise due to perpetual scaling of transistors. It has been found that the main reason behind this is non-scalable voltage due to the thermionic limit defined by Boltzmann for subthreshold slope (SS) in transistors, i.e., 60 mV/dec at room temperature [8-11]. Therefore, the viable solution to the problem of on-chip power and non-scalable voltage is to lower the SS of a transistor and overcome this fundamental limit of 60 mV/Dec.

For a decade, several new ways and architectures were provided by various researchers to overcome this scalability limit by reducing the SS below 60 mV/Dec. Numerous replacements were proposed by replacing conventional

transistors like Tunnel FETs, phase FETs, III-V silicon nanowires, and other modified structures to provide steep switching and energy-efficient scaling characteristics [12-16]. These amended FETs reduced the leakage current and provide good scaling capability by achieving a steep SS. On the other hand, degrading on-state characteristics and other crucial constraints such as ambipolar current and requirement of new fabrication processes [17-20], necessitates the need for a new transistor that can overcome the existing limit of SS and meet other performance parameters of transistors. In 2008, for the first time, the concept of Negative Capacitance FET (NCFET) was proposed by Salahuddin and Datta to meet the existing requirements in a transistor [21]. Since then, the NCFET has become a promising transistor due to its massive potential in disabling the fundamental limits of SS without compromising other performance parameters. Instead of these benefits, it also offers great compatibility with existing CMOS fabrication processes [22]. So, it is an extremely valuable alternative for conventional transistors. On this path, the NCFET reliably proved itself through various experimental and simulation-based studies [23-25] and acquired a new place in the semiconductor industry with emerging energy-efficient transistors.

This chapter discloses the various concepts, challenges, pros, and cons related to NCFET. Moreover, a thorough review of the role of NCFET in low-power applications has been provided and various future aspects related to NCFET have been discussed.

10.2 NCFET and Its Design Constraints

NCFET integrates a ferroelectric (FE) layer above the gate stack of an existing transistor, as shown in Figure 10.1. This ferroelectric material acts as negative capacitance under certain conditions [26]. This allows the transistor to provide the internal voltage amplification and comes up with a larger gain. Consequently, it achieves a desired drive current or on-state current (I_{on}) at a nominal supply voltage (V_{DD}) instead of a high-supply voltage, as shown in Figure 10.2 [27]. In return, it consumes low power and enables the attribute of sub-60 mV/decade of SS. Its compatibility with prevailing CMOS fabrication processes is a bonus that makes it highly efficient for emerging technologies in the semiconductor industry. This

simplifies the path for ultra-low power applications, even with sub-10 nm technology with existing fabrication processes [24-28]. Otherwise, the massive production of transistors with such a small dimension will never be possible.

The elegant simplicity and high scalability of the NCFET has encouraged many researchers in academia, as well as in industries, to explore the physics and technology behind it. They explored NCFET technology with different device structures for circuit and system levels [8, 22, 23]. The ferroelectric materials are rapidly used for the concept NC effect in devices, but there are various types of ferroelectric materials available, thus it is important to investigate which type of ferroelectric materials are compatible and useful with CMOS technology. So, NCFETs were predominantly explored for the different ferroelectric materials [29-31]. Further, these ferroelectric materials can be incorporated in FETs through two different types of structure. One of them is a Metal Ferroelectric Insulator Semiconductor (MFIS) in which the metal layer is directly deposited over the gate dielectric/insulator. In the other, i.e., a Metal Ferroelectric Metal Insulator Semiconductor (MFMIS), the ferroelectric layer is sandwiched between the two metal layers that act as a Metal Ferroelectric Metal (MFM) capacitor, which is added in series combination with the existing FETs [32, 33]. Both of these structures have their own features and influence on stability and electrical properties. Thus, the various studies on this NCFET device structure have been provided with different perspectives.

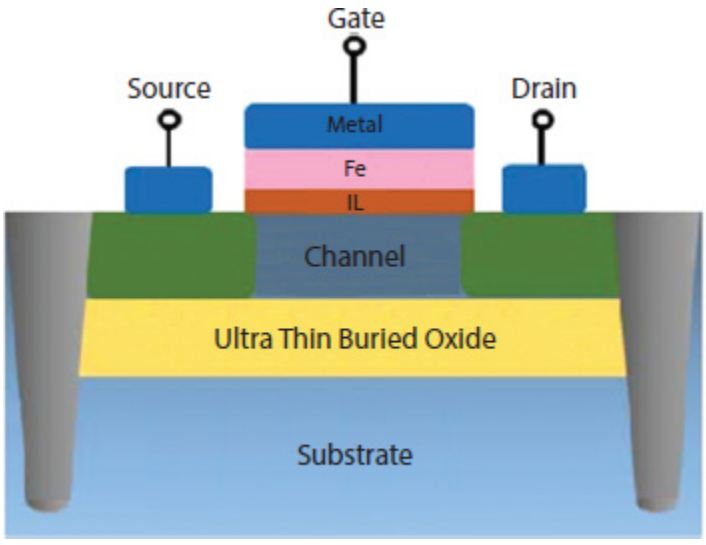

Figure 10.1 Basic structure of Negative Capacitance FET (NCFET) [26].

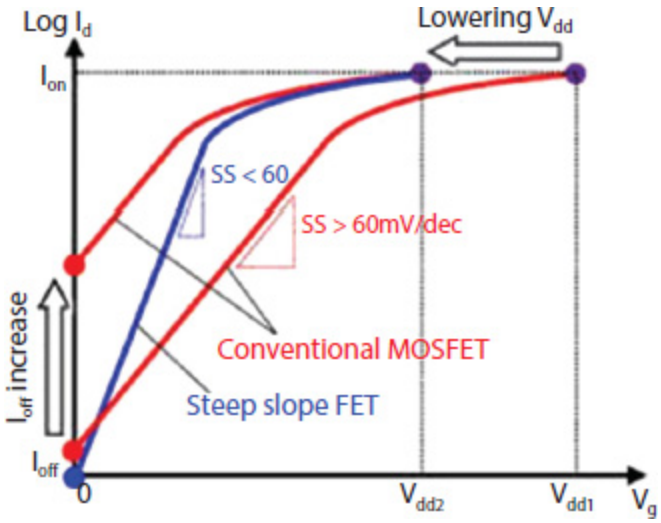

Figure 10.2 I-V characteristics of NCFETs vs. conventional MOSFETs [27].

Beyond these ferroelectric materials and device structure, another major concern related to NCFETs is their stability. As the name suggests negative capacitance, that means high charges at lower voltages (or $dQ/dV < 0$). High depolarizing fields in ferroelectrics gives rise to negative capacitance under the circumstances where the external electric field is unable to compensate the surface polarization charge [34]. So, it raises a question as to how it is stable under such circumstances. Consequently, the stability of NCFETs became a major concern. This stability in NCFETs depends on factors like hysteresis, capacitance matching, ferroelectric thickness, etc. In the last decade, various researchers have worked on these factors to achieve stability in NCFETs [34-37]. It has been found that a stable NCFET not only reduces SS below 60 mV/dec, but will result in negligible SCEs. Even some researchers revealed that NCFETs with proper capacitance matching result in Negative Drain Induced Barrier Lowering (DIBL) and Negative Drain Resistance (NDR) [38]. This type of transistor is an excellent choice for low-power applications. In the subsequent section of this section, we will discuss ferroelectric materials, device structure, compatibility, capacitance matching, and various simulative and experimental studies that investigated NCFET.

10.2.1 Ferroelectric Materials

Various types of ferroelectric materials were predominantly used in various applications such as sensors, capacitors, actuators, memory cells, and various energy storage devices. However, in the last decade, the NC effect in Ferroelectric material has attracted the attention of researchers for use in emerging semiconductor devices. Until 2016-17, perovskite and polymer-based ferroelectric materials such as $BiFeO_3$, PZT, PVD, and SBT were extensively employed for designing NCFETs [39-43], but these materials require a very thick layer up to 200nm to provide a negative capacitance effect. A thick layer above the gate stack may become vulnerable with extremely high gate capacitance [30], thus for circuit/system level design it shows instability, suffers from fatigue, and needs a high-quality epitaxy to integrate ferroelectric material in CMOS processes [31]. While moving towards short channel devices, it is nearly impossible to incorporate such a thick layer with compatible CMOS processes. Therefore, from 2015 onwards, researchers have moved towards hafnia based ferroelectric materials. In the year 2011, ferroelectricity was first noticed in doped HfO_2 materials to offer a negative capacitance effect even with a thin layer of ferroelectric material [44]. This hafnia-based material, mainly the HfO_2, is doped to achieve ferroelectric material with different dopants such as Silicon, Aluminum, Zirconium, Yttrium, Strontium, etc. [45]. These materials are highly compatible with CMOS processes. Moreover, while moving towards the circuit/system level design, hafnia based ferroelectric materials became a futuristic material for NC-based FETs. Thus, hafnia based NCFETs were broadly investigated for various FETs for their scalability, compatibility with CMOS processes, processing temperature tolerance limits, 3D-capable material, memories, circuit and system level design, and various other applications [46-50]. It was found that NCFETs with hafnia based ferroelectric materials can be successfully developed and demonstrate a very good device performance with proper capacitance matching. In the case of memories with proper tailoring, it meets the requirement of various memory applications [51]. Still, there are different hafnia based ferroelectric materials with different dopants. All these materials have their own properties related to stability, ferroelectricity, polarization, surface energy effect, etc. and these materials can be selected as per their requirements.

10.2.2 NCFET Structure

Negative capacitance exits in ferroelectric material under the circumstances where the external electric field is incapable of compensating the high depolarizing fields [52]. This type of capacitance is denoted as C_{FE} and, if deposited directly above the semiconductor, it becomes unstable. While considering it for various FETs, it turns out that it is important to make it stable for its appropriate performance. So, a positive capacitance has been added in series combination with it to stabilize its performance. For this purpose, two types of device structures, i.e., MFIS and MFMIS, are mainly used, as shown in Figure 10.3.

Both of these structures are investigated by the scholars and it is found that both have their own features and impact on ferroelectric characteristics [32, 33, 53]. M. Hoffmann *et. al* demonstrated that NCFETs with internal metal layers result in anti-parallel domain formation, which may cause hysteresis, and it is difficult to stabilize the NC State in this type of structure [53]. On the other side, G. Phawa *et. al*. elaborated that the MFMIS structure is relatively good compared to MFIS, with ferroelectric material having high remanent polarization at high supply voltages. For low remnant polarization materials however, the MFIS structures are more proficient at high supply voltages compared to MFMIS structures [33]. It has been also found that the fringing field persuades an equivalent electric field and polarization in MFMIS due to uniformly distributed charges [32]. Thus, the fringing field lines, along with S/D doping, have a resilient effect on the MFMIS compared to the MFIS structure. The entire energy barrier rises in MFMIS structure at high voltages, unlike in MFIS structure, and results in more negative DIBL. However, for short channels using gate spacers, the NC effect becomes more pronounced and results in steeper subthreshold slope on NCFETs and reduction in DIBL [54]. Another main factor that is investigated for both the device structures is leakage current as well as Gate Induced Drain Leakage (GIDL) current in NCFETs [55, 56]. It is revealed that MFMIS structures are much leakier than MFIS structures because of the existence of an inner layer of metal. Sometimes MFMIS becomes marginally stale or even much leakier than the baseline FETs. Hence, it is very important to choose the device structure carefully as per the ferroelectric material, hysteresis, application, and other requirements.

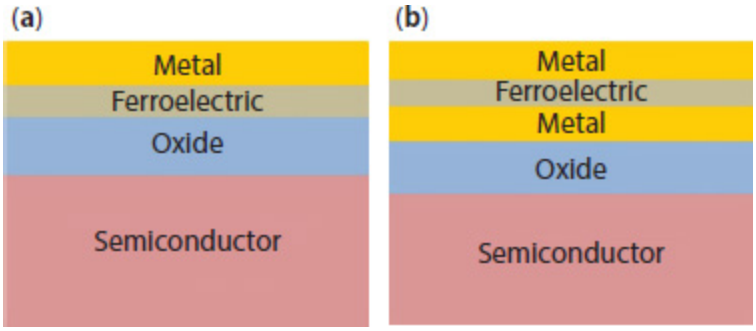

Figure 10.3 Types of NCFET structures: (a) Metal-Ferroelectric-Insulator-Semiconductor (MFIS) and (b) Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS).

10.2.3 Capacitance Matching and Ferroelectric Parameters

Another factor that is very important in the designing of NCFETs is capacitance matching. The C_{FE} is incorporated on the baseline FETs by selecting one of the two structures as per requirements. Still, there are some factors that have to be carefully considered for proper capacitance matching and stability of the device. One of them is the ferroelectric thickness, as it is known that capacitance is also dependent on the thickness of that material. Therefore, in the case of C_{FE}, the ferroelectric thickness, T_{FE}, becomes an important factor for device design. In the case of ferroelectric materials, the C_{FE} can be expressed as:

$$C_{FE} \approx \frac{-3.84 \times P_r}{T_{FE} \times E_C} \tag{10.1}$$

where P_r and E_C represent the ferroelectric remanent polarization and coercive electric field, respectively. These parameters are typically dependent on the inflection point of the material-dependent S-Curve [26]. Accordingly, the C_{FE} not only depends on the T_{FE} but also depends upon the P_r, E_C, and properties of the ferroelectric material. However, the doped HfO_2 materials persuade high values of polarization even with a thin layer and result in the NC effect. It is also considered a good material for proper capacitance matching. Still, the doping and type of dopant in HfO_2, thickness of the ferroelectric layer, effective gate oxide thickness, and other material-dependent parameters are imperative constraints. It is important to

optimize all these parameters for effective low-power NCFETs. It is observed that various researchers explored the NCFET with different thicknesses (T_{FE}) of different ferroelectric materials [47-50]. The results show that higher T_{FE} will provide high internal voltage amplification and a greater NC effect, which further provides a very steep subthreshold slope as well as more negative DIBL. This rise in T_{FE}, however, will lead to more hysteresis and the gate voltage will not amplify in the expected manner. This may also disturb the polarization, which further results in capacitance mismatching, a rise in delay, high leakage, and other timing constraints that are extremely detrimental for low-power applications [31, 57].

In the case of polarization, it has been exposed that ferroelectric with smaller P_r results has better capacitance matching in a weaker inversion region. This leads to enhanced gate control that results in low leakage characteristics, while ferroelectric with larger P_r results in better capacitance matching in strong inversion and better on-current characteristics, which are a good choice for RF applications [58]. Finally, in the case of the electric field, it is important to design a device in such a manner that it will not exceed the maximum allowable electric field along with a hysteresis-free operation [26]. This can be achieved when the device is designed by satisfying the conditions given below [17, 26]:

i. For a hysteresis-free and stable NC effect:

$$|C_{FE}| \geq C_{ins} \tag{10.2}$$

and

$$|C_{FE}| \geq C_{MOS} \tag{10.3}$$

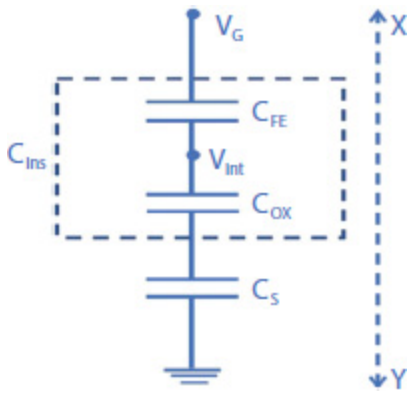

Figure 10.4 Equivalent capacitance model related to NCFETs [17].

where C_{ins} is a series combination of C_{FE} and C_{OX}. C_{OX} is defined as the capacitance across the gate dielectric and is expressed as:

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \tag{10.4}$$

where ε_{ox} and T_{ox} are the permittivity and physical thickness of the gate dielectric, respectively. C_{MOS} is the underlying MOSFET capacitance and is a series combination of C_{OX} and C_S. C_S is capacitance across the semiconductor. The equivalent capacitance model related to NCFETs is shown in Figure 10.4.

ii. To calculate the maximum allowable limit of the electric field:

$$|C_{FE}| = |C_{FE,\,Emax}| \tag{10.5}$$

where

$$C_{FE,Emax} = \frac{C_{ox}}{-1+\lambda}; \lambda = \frac{V_{DS} - V_{th}}{Q_{gmax} / C_{ox}} \tag{10.6}$$

where Q_{gmax} is total gate capacitance at $V_G = V_{DS}$ and V_{th} is the threshold voltage.

Thus, on sustaining the above-mentioned conditions, an NCFET having hysteresis free and stable NC effect and proper capacitance matching within the allowed electric field limit can be designed.

10.3 NCFET for Low-Power Applications

There is now a high requirement for a novel, CMOS-compatible and energy-efficient alternative for FETs and NCFET has shown its presence with high proficiency. Since then, it has been explored by using CMOS-compatible doped HfO_2-based ferroelectric materials with a distinct NCFET structure, ferroelectric thickness, and device architectures and some of them are tabulated in Table 10.1.

Table 10.1 Negative capacitance based different device structures and their performance parameters.

Basic device structure	Channel length	FE material	FE thickness (T_{FE})	Year	SS (mV/Dec)	Ref. no.
FDSOI	30 nm	Zr-HfO_2	1.8 nm	2019	20	[59]
MoS_2-FETs	500 nm	HZO	20 nm	2018	6.07	[60]
2D MoS2	2 µm	HZO	6 nm	2020	51.2	[61]
FinFET	22 nm	Doped-HfO_2	2 nm	2022	57	[62]
FinFET	30 nm	Doped-HfO_2	10 nm	2019	42	[63]
Gate-All-Around Finfet	sub-3 nm	HZO	3 nm	2022	< 25	[64]
Tunnel FET	50 nm	Doped-HfO_2	7 nm	2017	20	[65]
JL-Tunnel FET	50 nm	Si doped HfO_2	2.5 nm	2020	20	[66]
DG-JL FET	100 nm	HZO	0-12 nm	2020	Sub-60	[67]
GAA NC-JL-NWFET	20 nm	Al: HfO_2	4 nm	2019	30	[68]
NC-JL FinFET	14 nm	Si-HfO_2	2 nm	2021	56	[17]
DG-JLFET	1 µm	Si-HfO_2	10 nm	2016	10	[69]
FinFET	14 nm	HZO	3.6 nm	2019	48	[46]
GAA-FET	25 nm	HZO	5.5 nm	2018	22	[49]

These different NC-based FETs have shown extraordinarily steep SS up to 10 mV/Decade. It has also shown excellent performance even for sub-3nm of channel length. These NC based FETs have shown performance with minimal energy consumption with reverse SCEs [59-69]. NCFETs have shown efficient power performance with minimal SCEs and compatibility

with conventional CMOS fabrication processes. It became important to analyze for various low-power applications. Thus, it has been predominantly explored for various circuit and system-level designs. Further, it has been examined for various constraints that affect the performance of FETs such as process variabilities, temperature variations, etc. To understand the proper functioning of NCFETs, various models have also been developed. Thus, various details related to these NCFET-based circuit and system designs and the impact of process variations and various proposed analytical models have been discussed further in this chapter. The various future aspects related to NCFET have been elaborated at the end of chapter.

10.3.1 NCFET for Circuit and System Design

In this section, various applicable articles have been discussed related to circuit and system design using NCFET.

- **M. Rapp** *et. al*. (2019) examined NCFET based processors for trade-offs between their performance, cooling, frequency, and power [70]. It has been found that for NCFET's power-efficient performance, the circuits can be designed with two different methods. The first one uses the conventional supply voltage with increased frequency. The second one is to reduce the supply voltage by operating it on a conventional frequency. However, there will be a tradeoff between power and frequency because when frequency increases, the power will remain the same with the same supply voltage. Conversely, while reducing supply will definitely reduce power, the frequency will be a conventional frequency. Moreover, it offers better scaling compared to conventional processors by using dynamic voltage/frequency scaling (DVFS) techniques to provide a better tradeoff between both voltage and frequency. Additionally, an NCFET-based processor reduces the cooling cost compared to a conventional processor.
- **S.K. Samal** *et. al*. studied full chip power benefits with NCFETs [71]. A SPICE model was utilized with the well-calibrated NCFET model. They used the SPICE models by incorporating experimentally calibrated models of NCFETs. A polarization (P_o) of 6 μC/cm^2 and an electric field (E_C) of 0.7 MV/cm for a T_{FE} of 5 nm is experienced in

their work for a channel length of 20 nm. They revealed that an NCFET-based full chip with 70% of energy has been saved due to a reduction of V_{DD} from 0.8 V to 0.4 V with equivalent frequency performance compared to a baseline FET-based full chip. Additionally, an NCFET chip having the same V_{DD} is 44% faster than a conventional chip with a 3-4 % total power reduction.

- **S. Kaushal** *et. al*. studied the impact of scaling on NC-JL FinFET [24]. They considered the MFIS structure for NC-JL FinFET and scaled it for different technology nodes up to 5 nm of the technology node. It is revealed that the integration of negative capacitance (NC) with JL FinFET helps to reduce the leakage current and short channel effects such as sub-threshold slope and DIBL and provide high drive current, as well as fast switching, by reducing the intrinsic delay for an extremely short channel length compared to standard-JL FinFET even at 5 nm of the technology node. They have also analyzed it for GIDL current. It is observed that the GIDL current for NC-JL FinFET is a little bit higher compared to JL FinFET, but it is still within the considerable range for low-power applications. Further, it can be reduced by scaling the Fin Thickness as per specifications or requirements.
- **Y.-K. Lin** *et. al*. worked on spacer engineering in NC FinFET [72]. In short channel devices, the fringing fields are an important concern. The outer fringing field is fine with the spacers. It impacts not only the gate capacitance but also the drain current. Thus, different spacer configurations are examined for the performance of NC-FinFET. Various spacer configurations such as air, fin selective, fin corner, full, and dual, are shown in Figure 10.5. They revealed that NC-FinFET requires the fin selective and full spacer for better capacitance matching.

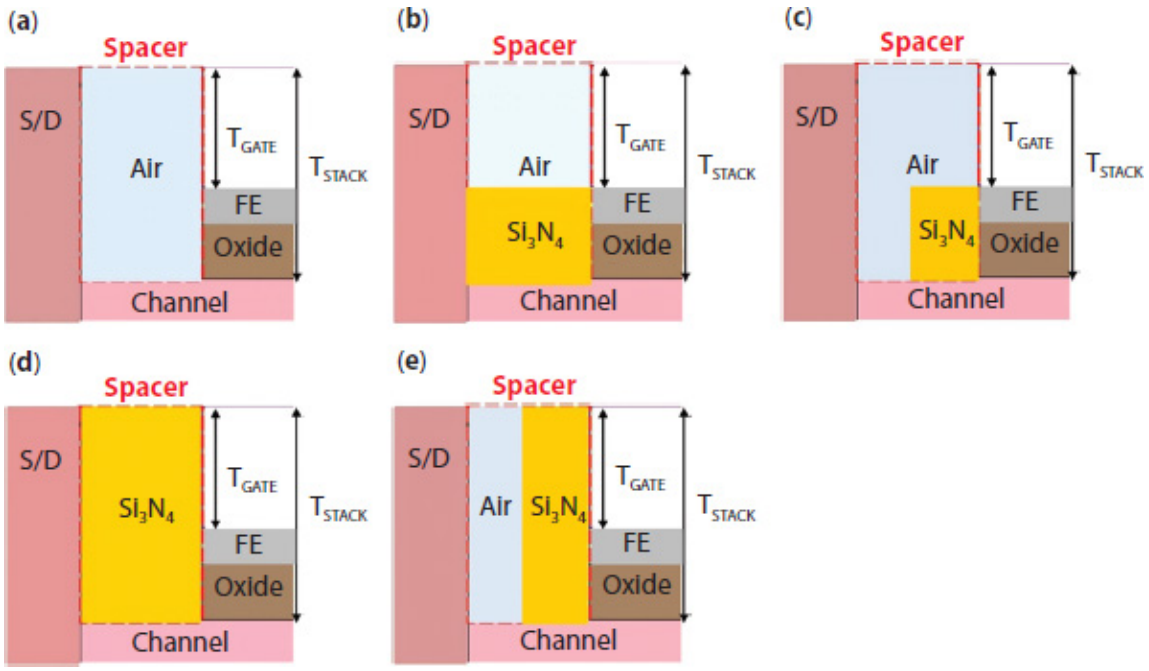

Figure 10.5 Distinct spacer configurations: (a) Air, (b) Fin Selective, (c) Fin Corner, (d) Full, (e) Dual (used in [72] to examine their impact on NC FinFET).

- Similarly, the impact of these spacer configurations is also investigated for NC-JL FET with a multigate structure [73]. It has been demonstrated that among various spacer configurations, a full spacer configuration has shown better results for NC-MGJL FET.
- The GIDL current is an important factor for low-power applications. The NC-FinFET has shown excellent performance for low power applications with negative DIBL, NDR, steep SS, etc., but it is important to analyze for GIDL current. Thus, **A. D. Gaidhane** *et. al.* examined the NC-FinFET for GIDL current. [74]. The NC FinFET considered in this work is based on an MFIS structure with a T_{FE} of 3 nm. They stated that due to steeper energy band profiles near the source and drain side in NCFET there is a larger onset of longitudinal band-to-band tunneling (L-BTBT) current compared to the baseline FinFET. This raises the tunneling in the gate-drain overlapped region, which contributes to the rise in GIDL current in the NC FinFET. There is an effective rise in GIDL current with the increase in T_{FE}, as shown in Figure 10.6. Thus, they summarized that there is an urgent need to

find an effective method to reduce the GIDL in NCFETs for better low-power characteristics.

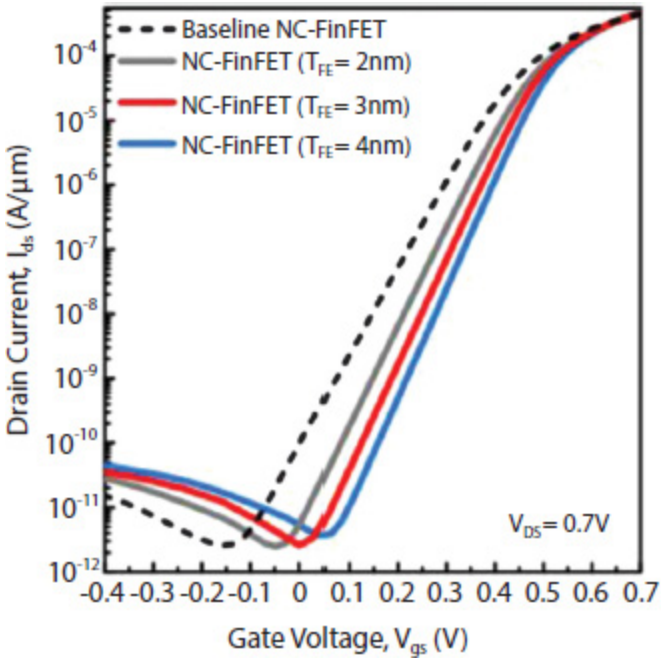

Figure 10.6 Variation of GIDL current with ferroelectric thickness in NC-FinFET [74].

- **Again in 2020, A. D. Gaidhane** *et. al*. examined the NC nanosheet FET (NC-NSFET) for a digital circuit with an inverter and inverter based 6T SRAM [75]. This NC-NSFET has a GAA structure and has been explored for different thicknesses of ferroelectricity. The NC-NSFET inverter provides steep Voltage Transfer Characteristics (VTC) with little hysteresis. In the case of SRAM, it provides high stability in the HOLD and READ state due to high drain current.
- **F. Bellando** *et. al* proposed subharmonic NCFET as an Ion Sensitive Field Effect Transistor (ISFET) [76]. They experimentally demonstrated that the NCFET enables subharmonic operation for ISFET, which enhance its applications for highly sensitive and low-power sensors. This NCFET-based ISFET with sub-thermionic operation offers a steep SS of 20mV/decade over two decades with Si-doped HfO_2 as a ferroelectric material. By observing its tremendous performance, they uncovered that the NCF*ET al*so opens up a door with a huge scope for low-power sensor applications.

- Recently, **S. Salamin** *et. al*. presented a breakthrough in Neural Networks (NNs) that led to significant accuracy improvements of several machine learning applications such as image classification and voice recognition [77]. A full chip for the computational core of a Google-based Tensor Processing Unit (TPU) has been designed using more than 4000 14nm NC-FinFETs. As NC FinFET delivers 2.8x higher efficiency compared to the conventional FinFET baseline, the NC FinFET-based TPU mitigates the issue of excessive on-chip heat which reduces the number of hot spots and hence relaxes the requirement of advanced cooling methods. They concluded that the NC-FinFET based in cost-effective TPU for neural network applications by minimizing the cooling cost realizes as well as delivers high efficiency compared to baseline FinFET based TPU.
- Moreover, recently in 2022, B. Awadhiya *et. al*. explored the effect of body biasing on the performance of NCFET [78]. They revealed that in an n-type of NCFET, the leakage current reduces while the threshold voltage increases with a rise in body biasing. On the other side, an increase in negative body biasing reduces the threshold voltage and raises the leakage current. The body factor found for NCFET is negative, while it is positive in conventional MOSFET. It has been found that body biasing in NCFET is beneficial for digital circuit design.

Numerous experimental as well as simulation-based works have shown that NCFET is highly beneficial for low-power applications. It can be scaled efficiently by using the DVFS technique. These NCFETs show efficient power performance even at 3nm and 5nm of channel length. That will make it a futuristic candidate for various low-power applications. The only parameter that needs to be focused for low-power applications is Gate Induced Drain Leakage Current. This can be reduced effectively by making minute changes in the device dimensions.

10.3.2 Impact of Process Variations on NCFET

However, these NCFETs have made highly efficient circuits and systems and the presence of new materials will introduce various process variations in the device. Therefore, it is important to analyze the impact of

temperature, trap charges, variability, and other process dependent parameters on the performance of NCFETs. Various scholars have examined the impact of these variations on different NC-based device structures. We cover related works and future aspects related to these process variations in this section.

Impact of Interface Traps: T. Kim *et. al*. observed that in NCFET with MFM structure, the transient response can be reinforced due to the presence of interface traps [79]. In the case of 2D NCFET and NC-FDSOI FET, the interface traps degrade the SS, current characteristics, and other performance parameters for low power applications [80, 81]. However, the performance of NC-FinFET is not affected much due to interface traps and are less sensitive to this type of variability [82].

Impact of Process Variations: In 2020, Hussam Amrouch *et. al*. also studied the impact of variability in device design parameters on the performance of MFMIS NC-FinFET [83]. They considered the variations for the ferroelectric layer as well as for the baseline transistor, as well as variations in ferroelectric layer thickness, coercive field, polarization, channel length, effective oxide thickness, gate work function, fin thickness, fin height, etc. They revealed that the induced process variations may affect the delay and frequency as well as gain performance of the device. So, it is important to consider process variations to correctly estimate the actual benefits of NC-FinFET. T. Dutta *et. al*. studied the impact of variations in ferroelectric parameters on NC FinFET [84]. The variability with ferroelectric parameters does not affect the performance of the threshold voltage and drain current in NC-FinFET. If an NC-FinFET exhibits the proper capacitance matching and stability, then it is highly immune to variability in ferroelectric parameters and results in reverse SCEs. It will also reduce the delay variability in NC-CMOS based ring oscillators. Similarly, C. Lin *et. al*. also worked on the variation of ferroelectric properties and their impact on device performance [85]. They considered a ±3% of variation in the NCFETs which does not affect the hysteresis and will also cause a considerable variation in the performance of the device. Recently, a 7 nm NC FinFET based SRAM is also investigated by including these process variations [86]. They have considered the gate work function variability and ferroelectric thickness variability. To find the impact of these variabilities they considered various figures of merit like threshold voltage,

current, gain, stability margins, etc. It has shown that the NC-FinFET based SRAM are less prone to variability compared to the FinFET based SRAM due to a Negative DIBL and NDR effect. Thus, the NC-FinFET based SRAM enables supply voltage scaling. Still, it is important to consider the variabilities induced due to various processes as they can diminish the abundant benefits achieved due to the NC effect.

Impact of Temperature Variations: C. Wang *et. al*. studied the impact of temperature on the performance of NCFET that have HZO as ferroelectric material [87]. They revealed that at room temperature the NCFET exhibits much better electrical performance compared to MOSFET in terms of SS and current, but when the temperature is increased from 25ºC to 85**ºC, in** the subthreshold region the current increases with rise in temperature and reduces in the overdrive with rise in temperature. The SS is increasing significantly with the rise in temperature. Increasing the rate for SS is slow at small temperatures and high at large temperatures, but still the SS and current characteristics are better than the baseline MOSFET even at high temperatures. J. Jo and C. Shin also investigated the effect of temperature on NCFET and developed a temperature-dependent equation of internal voltage gain, as given below [88]:

$$\frac{\partial V_{int}}{\partial V_G} \sim \frac{C_{FE}(T)}{C_{FE}(T)+C_S} \tag{10.7}$$

where the $\frac{\partial V_{int}}{\partial V_G}$ is internal voltage gain and C_{FE} and C_S is the capacitance of the ferroelectric layer and MOS transistor. It is well known that the internal voltage amplification is dependent on gain and hence on the temperature. With an increase in temperature, there is a reduction in internal voltage gain and hence it reduces the internal voltage amplification. This will lead to an increase in SS with the increase in temperature. Moreover, in 2021, Om Prakash *et al*. investigated the impact of self-heating effects (SHEs) on the performance of NC FinFET [89]. It has been found that the SHE is dominant for both FinFET and NC FinFET for high frequency applications and degrades the ON current at high V_{DS}. The ON current is high in NC FinFET compared to FinFET, therefore the SHE is more dominant in NC FinFET at high V_{DS} compared to FinFET. While in a weak

inversion region or at low V_{DS}, the SHE is negligible and well considered for low-power applications. Thus, it can be said that the impact of varying temperature on the performance of NCFET is considerable for low-power applications.

The impact of various process dependent variations on the performance of different NCFET structures has been investigated effectively and the impact of temperature and interface traps has been investigated individually on different devices. Their collective impact on the same device has not been investigated yet. Moreover, the FETs considered in these studies are mostly NC-based MOSFET, FinFET, and 2D FET. While the impacts of these variations are still unknown for NC-based TFET, Junctionless FET, and other device structures. Additionally, the impact of various other process parameters or variations such as Hot Carrier Injection (HCI), Line Edge Roughness (LER), Random Doping Fluctuations (RDF), Oxide Thickness Variation (OTV), etc. needs to be considered in NC-based FETs.

10.3.3 Analytical Models for NCFET

The NC-based FETs are a tremendous choice for future low-power applications and are also less prone to process variabilities compared to conventional FETs. So, it is also important to understand how the NC effects the charge and capacitance behavior of the FETs that eventually perform internal voltage amplification. Thus, various researchers developed physics-based analytical or compact models for different NC-based device structures.

Initially, in 2010, David Jiménez *et. al*. developed an analytical model for the surface potential and drain current in NCFET. This model is mainly focused on low-power switching characteristics and operation of the NC region. In their work, a long channel MFIS NCFET was considered with a conventional SBT as ferroelectric material [90]. In 2016, C. Jiang *et. al*. developed an analytical model for long-channel NC GAA FET with an MFIS structure [91]. SBT was used as the ferroelectric material and the model was developed for drain current, gain, and various SCEs. Later on, doped HfO_2 came into consideration. In the year 2017, a compact model for MFIS NCFET was developed [92]. The model includes gate charge density and the drain current's weak inversion as well as in strong inversion

regions. It has been also analyzed for the effect of variations in ferroelectric parameters on the performance of both MFIS and MFMIS NCFET. Further, an analytical model for drain current, charges, and capacitances in NC-GAA FETs has been developed [93]. In this work, the structure considered was MFIS and this model was applicable only for long channel devices. Again, a compact model for a GAA NC MFIS transistor including the radial dependence of the electric field in the ferroelectric layer was proposed [75]. They revealed that the GAA-NCFET does not change its off-current and drain saturation compared to GAA-FET. For high drain bias, the gate terminal charge for GAA-NCFET was found to saturate to 4/5 of the maximum value, while it saturates to 2/3 of the maximum value in the case of GAA-FET. They neglected the damping effect of ferroelectric material on GAA-NCFET, which in turn affects the performance of the device. R. Liang *et al*. and C.K. Dabhi *et al*. also proposed the models for surface potential, drain current, and circuit simulations to understand the physics behind NCFETs [94, 95]. A small signal model was also proposed for NCFET and analyzed for analog applications [96]. They utilized various combinations like T, **π** to develop a model for various parameters like gain, input/output capacitance, frequency, and bandwidth. In 2020, N. Pandey *et al*. developed a model for MFIS structure based NCFETs for short channel effects [97]. The Green's function approach has been used with an L-K equation in this model for a subthreshold region. A double gate NCFET was under consideration in this work. The model developed is a 2D model including distinct quantum-mechanical effects. Further, an analytical model for NC based double gate FET was also developed by taking interface trap charges and temperature effects into account [98]. But while taking a short channel device into consideration, it is equally important to consider the fringing field effect while developing a model. Otherwise, it will lead to an inaccurate model. Y.K. Lin *et. al*. proposed a model for NCFET by including the effect of inner fringing fields [99]. It has been found that the inner fringing field does not affect the performance of long-channel devices. For short channel devices at 7/8-nm of technology node, the inner fringing field suppresses the SCEs as well as enhances the performance of the device. In 2021, an analytical model for subthreshold voltage for an MFIS type of NC-JL FinFET has been developed by including both inner and outer fringing field effects for a short channel device [100]. It has been found that the increase in spacer length reduces the fringing field

capacitance, which may lead to an increase in the threshold voltage of the device. Further, this model was extended for subthreshold drain current and various SCEs like SS and DIBL for low-power applications [101]. In this model, the drift-diffusion equation was used to calculate the drain current in the device. Another parameter which is important to consider low power applications is GIDL current. Due to steeper band edges in NCFET, the GIDL current increases drastically and may lead to an increase power dissipation. Recently, an analytical model for GIDL current in NC-JL FinFET has been developed [102]. The GIDL current in NC-JL FinFET was analyzed with varying device design parameters such as ferroelectric thickness, fin height, fin thickness, etc. The trade-off between these design parameters has been proposed to effectively minimize the GIDL current for low-power applications.

Various models were developed for NC-based FETs for low-power as well as analog applications, but most of these models are developed for MFIS-based structures. While the MFMIS structures are equally important, it is essential to develop an analytical model for MFMIS structure. Most of these models have ignored the effect of fringing fields, trap charges, temperature, etc., so there is a need to include all these ultra-short channel effects while developing a model for NCFET.

10.4 Summary

Since the possibility of existence of a negative capacitance has been realized, the NCFETs have been examined extensively for low-power applications. This concept of having the NC effect with the addition of a thin ferroelectric layer can make a dramatic change in the semiconductor industry. Additionally, after observing this effect in CMOS compatible HfO_2 based ferroelectric material, NCFET facilitates as a new CMOS compatible futuristic technology. Since then, various NCFET based circuits, chips, processors, TPU, etc. have been investigated using different structures based on NCFET technology. Various methods have been offered to deal with the problem of hysteresis, capacitance matching, and stability of the NC effect. Due to the high scope of NCFET in future technologies, it is important to explore some other aspects related to it. A few of them are addressed below:

- The NC-FinFET has shown a great scope in low-power applications, but mostly the NC-FinFET is analyzed for a single fin structure. However, for low power logic/mixed signal circuits, there is a need for multi-fin structures. So, it is high time to investigate multi-fin structures in addition to the NC effect.
- However, the NCFET needs to be investigated for various other issues related to process variations and aging of transistors such as Hot Carrier Injection (HCI), Positive / Negative Bias Temperature Instability (PBTI/ NBTI), quantum confinement effects, LER, OTV, RDF, etc. for their better functionality, reliability, and longer life.
- The NCFET has been explored for various low-power applications, but there is a lack of clear design insights to make an energy-efficient and secure network/hardware.
- The NCFET has been predominantly explored for low-power applications, but due to its internal voltage amplifications it can be beneficial for RF/analog and sensor applications and needs to be explored.

References

[1] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, “Design of ion-implanted MOSFET’s with very small physical dimensions,” *IEEE Journal of Solid-State Circuits*, vol. 9, no. 5, pp. 256-268, 1974.

[2] O. Semenov, A. Vassighi, M. Sachdev, A. Keshavarzi, and C. F. Hawkins, “Effect of cmos technology scaling on thermal management during burn-in,” *IEEE Transactions on Semiconductor Manufacturing*, vol. 16, no. 4, pp. 686– 695, Nov-2003.

[3] S. Salahuddin, K. Ni, and S. Datta, “The era of hyper-scaling in electronics,” *Nature Electronics*, vol. 1, no. 8, pp. 442–450, 2018.

[4] T. W. Kenny, K. E. Goodson, J. G. Santiago, E. Wang, J.-M. Koo, L. Jiang, E. Pop, S. Sinha, L. Zhang, D. Fogg, S. Yao, R. Flynn, C.-H. Chang, And C. H. Hidrovo, “Advanced Cooling Technologies for

Microprocessors," *International Journal of High Speed Electronics and Systems*, vol. 16, no. 01, pp. 301–313, 2006.

[5] S. M. Sohel Murshed and C. A. Nieto de Castro, "A critical review of traditional and emerging techniques and fluids for electronics cooling," *Renewable and Sustainable Energy Reviews*, vol. 78, pp. 821–833, 2017.

[6] S. Wang, Y. Yin, C. Hu, and P. Rezai, "3D Integrated Circuit Cooling with Microfluidics," *Micromachines*, vol. 9, no. 6, p. 287, 2018.

[7] "*Inventory of U.S. Greenhouse Gas Emissions and Sinks*" United States Environmental Protection Agency, EPA FY 2020, US. [Online]. Available: https://www.epa.gov/ghgemissions/inventory-us-greenhouse-gas-emissions-and-sinks. [Accessed: 05-Aug-2022].

[8] S. B. Rahi, S. Tayal, and A. K. Upadhyay, "A review on emerging negative capacitance field effect transistor for low power electronics," *Microelectronics Journal*, vol. 116, p. 105242, Oct-2021.

[9] S. K. Moore, "*Another step toward the end of Moore's law: Samsung and TSMC move to 5-nanometer manufacturing* - [News]," in IEEE Spectrum, vol. 56, no. 6, pp. 9-10, 2019.

[10] *International Technology Roadmap for Semiconductors*, ITRS 2.0, 2013. [Online]. Available: http://public.itrs.net. [Accessed: 05-Aug-2022].

[11] Y. Taur and T. Ning, *Fundamentals of modern VLSI design*. UK, Cambridge University Press, 1998.

[12] J. Frougier, N. Shukla, D. Deng, M. Jerry, A. Aziz, L. Liu, G. Lavallee, T. S. Mayer, S. Gupta, and S. Datta, "Phase-Transition-FET exhibiting steep switching slope of 8mV/decade and 36% enhanced ON current," *IEEE Symposium on VLSI Technology*, 2016, pp. 1-2.

[13] C. Wu, R. Huang, Q. Huang, J. Wang, and Y. Wang, "Design Guideline for Complementary Heterostructure Tunnel FETs With Steep Slope and Improved Output Behavior," *IEEE Electron Device Letters*, vol. 37, no. 1, pp. 20-23, 2016.

[14] K. Tomioka, M. Yoshimura, E. Nakai, F. Ishizaka, and T. Fukui, “Integration of III-V nanowires on Si: From high-performance vertical FET to steep-slope switch,” *IEEE International Electron Devices Meeting*, 2013, pp. 1-4.

[15] S. B. Rahi, P. Asthana, and S. Gupta, “Heterogate junctionless tunnel field-effect transistor: future of low-power devices,” *Journal of Computational Electronics*, vol. 16, no. 1. pp. 30–38, 2016.

[16] S. B. Rahi, B. Ghosh, and B. Bishnoi, “Temperature effect on hetero structure junctionless tunnel FET,” *Journal of Semiconductors*, vol. 36, no. 3, p. 034002, 2015.

[17] S. Kaushal and A. K. Rana, “Negative Capacitance Junctionless FinFET for Low Power Applications: An Innovative Approach,” *Silicon*, 2021.

[18] G. N, R. SB, and L. M, “Suppression of Ambipolar Current and Analysis of RF Performance in Double Gate Tunneling Field Effect Transistors for Low-Power Applications,” *International Journal of Nanoparticles and Nanotechnology*, vol. 6, no. 1, 2020.

[19] O. Knopfmacher, D. Keller, M. Calame, and C. Schönenberger, “Dual Gated Silicon Nanowire Field Effect Transistors,” *Procedia Chemistry*, vol. 1, no. 1, pp. 678–681, 2009.

[20] A. A. Leonardi, M. J. L. Faro, and A. Irrera, “Silicon Nanowires Synthesis by Metal-Assisted Chemical Etching: A Review,” *Nanomaterials*, vol. 11, no. 2, p. 383, 2021.

[21] S. Salahuddin and S. Datta, “Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices,” *Nano Letters*, vol. 8, no. 2, pp. 405-410, 2008.

[22] L. Tu, X. Wang, J. Wang, X. Meng, and J. Chu, “Ferroelectric Negative Capacitance Field Effect Transistor,” *Advanced Electronic Materials*, vol. 4, no. 11, p. 1800231, 2018.

[23] M. A. Alam, M. Si and P. D. Ye, “A critical review of recent progress on negative capacitance field-effect transistors,” *Applied Physics Letters*,

vol. 114, no. 9, p. 090401, 2019.

[24] S. Kaushal, A. K. Rana, and R. Sharma, “Performance Evaluation of Negative Capacitance Junctionless FinFET under Extreme Length Scaling,” *Silicon*, vol. 13, no. 10, pp. 3681–3690, 2021.

[25] S. Tayal, A. Kumar, D. Kumar, and S. B. Rahi, *Emerging low-power semiconductor devices: Applications for future technology nodes*. Boca Raton: CRC Press, 2022.

[26] H. Agarwal, P. Kushwaha, Y.-K. Lin, M.-Y. Kao, Y.-H. Liao, J.-P. Duarte, S. Salahuddin, and C. Hu, “NCFET Design Considering Maximum Interface Electric Field,” *IEEE Electron Device Letters*, vol. 39, no. 8, pp. 1254-1257, 2018.

[27] K. Jang, T. Saraya, M. Kobayashi and T. Hiramoto, “Ion/Ioff ratio enhancement and scalability of gate-all-around nanowire negative-capacitance FET with ferroelectric HfO_2,” *Solid-State Electronics*, vol. 136, pp. 60-67, 2017.

[28] H. W. Cho, P. Pujar, M. Choi, S. Kang, S. Hong, J. Park, S. Baek, Y. Kim, J. Lee, and S. Kim, “Direct growth OF orthorhombic HF0.5ZR0.5O2 thin films for hysteresis-free MoS2 negative capacitance field-effect transistors,” *npj 2D Materials and Applications*, vol. 5, no. 46, pp. 1-8, 2021.

[29] L. W. Martin and A. M. Rappe, “Thin-film ferroelectric materials and their applications,” *Nature Reviews Materials*, vol. 2, no. 2, 2016.

[30] F. A. McGuire, Z. Cheng, K. Price, and A. D. Franklin, “Sub-60 mV/decade switching in 2D negative capacitance field-effect transistors with integrated ferroelectric polymer,” *Applied Physics Letters*, vol. 109, no. 9, p. 093101, 2016.

[31] T. Mikolajick, S. Slesazeck, H. Mulaosmanovic, M. H. Park, S. Fichtner, P. D. Lomenzo, M. Hoffmann, and U. Schroeder, “Next generation ferroelectric materials for semiconductor process integration and their applications,” *Journal of Applied Physics*, vol. 129, no. 10, p. 100901, 2021.

[32] G. Pahwa, A. Agarwal, and Y. S. Chauhan, “Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior,” *IEEE Transactions on Electron Devices*, vol. 65, no. 11, pp. 5130–5136, 2018.

[33] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, “Physical Insights on Negative Capacitance Transistors in Non-hysteresis and Hysteresis Regimes: MFMIS versus MFIS Structures,” *IEEE Transactions on Electron Devices*, vol. 65, no. 3, pp. 867–873, 2018.

[34] J. Íñiguez, P. Zubko, I. Luk’yanchuk, and A. Cano, “Ferroelectric negative capacitance,” *Nature Reviews Materials*, vol. 4, no. 4, pp. 243–256, 2019.

[35] A. Jain and M. A. Alam, “Stability Constraints Define the Minimum Subthreshold Swing of a Negative Capacitance Field-Effect Transistor,” *IEEE Transactions on Electron Devices*, vol. 61, no. 7, pp. 2235–2242, 2014.

[36] H. Wang, M. Yang, Q. Huang, K. Zhu, Y. Zhao, Z. Liang, C. Chen, Z. Wang, Y. Zhong, X. Zhang, and R. Huang, “New Insights into the Physical Origin of Negative Capacitance and Hysteresis in NCFETs,” *2018 IEEE International Electron Devices Meeting (IEDM)*, 2018.

[37] J. Jo and C. Shin, “Negative Capacitance Field Effect Transistor With Hysteresis-Free Sub-60-mV/Decade Switching,” *IEEE Electron Device Letters*, vol. 37, no. 3, pp. 245–248, 2016.

[38] T. Yu, W. Lü, Z. Zhao, P. Si, and K. Zhang, “Negative drain-induced barrier lowering and negative differential resistance effects in negative-capacitance transistors,” *Microelectronics Journal*, vol. 108, p. 104981, 2021.

[39] G. A. Salvatore, A. Rusu, and A. M. Ionescu, “Experimental confirmation of temperature dependent negative capacitance in ferroelectric field effect transistor,” *Applied Physics Letters*, vol. 100, no. 16, p. 163504, 2012.

[40] A. Rusu, A. Saeidi, and A. M. Ionescu, “Condition for the negative capacitance effect in metal–ferroelectric–insulator–semiconductor

devices," *Nanotechnology*, vol. 27, no. 11, p. 115201, 2016.

[41] A. I. Khan, K. Chatterjee, J. P. Duarte, Z. Lu, A. Sachid, S. Khandelwal, R. Ramesh, C. Hu, and S. Salahuddin, "Negative Capacitance in Short-Channel FinFETs Externally Connected to an Epitaxial Ferroelectric Capacitor," *IEEE Electron Device Letters*, vol. 37, no. 1, pp. 111–114, 2016.

[42] E. Ko and C. Shin, "Effective drive current in steep slope FinFET (vs. conventional FinFET)," *Applied Physics Letters*, vol. 111, no. 15, p. 152105, 2017.

[43] A. Saeidi, F. Jazaeri, F. Bellando, I. Stolichnov, G. V. Luong, Q.-T. Zhao, S. Mantl, C. C. Enz, and A. M. Ionescu, "Negative capacitance as performance booster for tunnel FETs and MOSFETs: An experimental study," *IEEE Electron Device Letters*, vol. 38, no. 10, pp. 1485–1488, 2017.

[44] J. Müller, T. S. Böscke, U. Schröder, S. Mueller, D. Bräuhaus, U. Böttger, L. Frey, and T. Mikolajick, "Ferroelectricity in Simple Binary ZrO2 and HfO2," *Nano Letters*, vol. 12, no. 8, pp. 4318–4323, 2012.

[45] J. Müller, P. Polakowski, S. Mueller, and T. Mikolajick, "Ferroelectric hafnium oxide based materials and devices: Assessment of current status and future prospects," *ECS Journal of Solid State Science and Technology*, vol. 4, no. 5, 2015.

[46] W. You, P. Su, and C. Hu, "Evaluation of NC-FinFET Based Subsystem-Level Logic Circuits," *IEEE Transactions on Electron Devices*, vol. 66, no. 4, pp. 2004-2009, 2019.

[47] Y. Zhao, Z. Liang, Q. Huang, C. Chen, M. Yang, Z. Sun, K. Zhu, H. Wang, S. Liu, T. Liu, Y. Peng, G. Han, and R. Huang, "A Novel Negative Capacitance Tunnel FET With Improved Subthreshold Swing and Nearly Non-Hysteresis Through Hybrid Modulation," *IEEE Electron Device Letters*, vol. 40, no. 6, pp. 989-992, 2019.

[48] S. Wang, X. Chen, Y. Pan, Q. Jia, Y. Yin, Y. Wu, Y. Wang, and W. Li, "Design of negative capacitance tunneling field effect transistor with dual-source U-shape channel, super-steep subthreshold swing and large

on-state current," *Superlattices and Microstructures*, vol. 155, p. 106905, 2021.

[49] M. H. Lee, K.-T. Chen, C.-Y. Liao, S.-S. Gu, G.-Y. Siang, Y.-C. Chou, H.-Y. Chen, J. Le, R.-C. Hong, Z.-Y. Wang, S.-Y. Chen, P.-G. Chen, M. Tang, Y.-D. Lin, H.-Y. Lee, K.-S. Li, and C. W. Liu, "Extremely steep switch of negative-capacitance nanosheet GAA-FETs and FinFETs," *IEEE International Electron Devices Meeting (IEDM)*, 2018.

[50] S.-Y. Lee, H.-W. Chen, C.-H. Shen, P.-Y. Kuo, C.-C. Chung, Y.-E. Huang, H.-Y. Chen, and T.-S. Chao, "Experimental Demonstration of Performance Enhancement of MFMIS and MFIS for 5-nm × 12.5-nm Poly-Si Nanowire Gate-All-Around Negative Capacitance FETs Featuring Seed-Layer and PMA-Free Process," in *Proc. 2019 Silicon Nanoelectronics Workshop (SNW)*, 2019, pp. 1-2.

[51] Z. Fan, J. Chen, and J. Wang, "Ferroelectric HfO2-based materials for next-generation ferroelectric memories," *Journal of Advanced Dielectrics*, vol. 06, no. 02, p. 1630003, 2016.

[52] M. Hoffmann, P. V. Ravindran, and A. I. Khan, "Why Do Ferroelectrics Exhibit Negative Capacitance?," *Materials*, vol. 12, no. 22, p. 3743, 2019.

[53] M. Hoffmann, M. Pešić, S. Slesazeck, U. Schroeder, and T. Mikolajick, "On the stabilization of ferroelectric negative capacitance in nanoscale devices," *Nanoscale*, vol. 10, no. 23, pp. 10891–10899, 2018.

[54] J. Hattori, K. Fukuda, T. Ikegami, H. Ota, S. Migita, H. Asai, and A. Toriumi, "Fringing field effects in negative capacitance field-effect transistors with a ferroelectric gate insulator," *Japanese Journal of Applied Physics*, vol. 57, no, p. 04FD07, 2018.

[55] A. I. Khan, U. Radhakrishna, S. Salahuddin, and D. Antoniadis, "Work Function Engineering for Performance Improvement in Leaky Negative Capacitance FETs," *IEEE Electron Device Letters*, vol. 38, no. 9, pp. 1335-1338, 2017.

[56] J. Min, G. Choe, and C. Shin, "Gate-induced drain leakage (GIDL) in MFMIS and MFIS negative capacitance FinFETs," *Current Applied*

Physics, vol. 20, no. 11, pp. 1222–1225, 2020.

[57] Y. Liang, X. Li, S. K. Gupta, S. Datta, and V. Narayanan, “Simulation-based study of negative capacitance double-gate junctionless transistors with a Compact SPICE Model,” *IEEE Transactions on Electron Devices*, vol. 65, no. 12, pp. 5525-5529, 2018.

[58] T. Yu, W. Lü, Z. Zhao, P. Si, and K. Zhang, “Effect of different capacitance matching on negative capacitance FDSOI transistors,” *Microelectronics Journal*, vol. 98, p. 104730, 2020.

[59] D. Kwon, S. Cheema, N. Shanker, K. Chatterjee, Y.-H. Liao, A. J. Tan, C. Hu, and S. Salahuddin, “Negative Capacitance FET With 1.8-nm-Thick Zr-Doped HfO2 Oxide,” *IEEE Electron Device Letters*, vol. 40, no. 6, pp. 993–996, 2019.

[60] M. Si, C.-J. Su, C. Jiang, N. J. Conrad, H. Zhou, K. D. Maize, G. Qiu, C.-T. Wu, A. Shakouri, M. A. Alam, and P. D. Ye, “Steep-slope hysteresis-free negative capacitance MoS2 transistors,” *Nature Nanotechnology*, vol. 13, no. 1, pp. 24–28, 2017.

[61] S. Zhang, Y. Liu, J. Zhou, M. Ma, A. Gao, B. Zheng, L. Li, X. Su, G. Han, J. Zhang, Y. Shi, X. Wang, and Y. Hao, “Low Voltage Operating 2D MoS2 Ferroelectric Memory Transistor with Hf1-xZrxO2 Gate Structure,” *Nanoscale Research Letters*, vol. 15, no. 1, 2020.

[62] M. Sil, S. M. Nawaz, and A. Mallik, “On the performance of hafniumoxide-based negative capacitance FinFETs, with and without a spacer,” *Semiconductor Science and Technology*, vol. 37, no. 4, p. 045006, 2022.

[63] X. Xu, J. Hu, and S. Ke, “Negative Capacitance Dual-Threshold Independent Gate FinFETs,” *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019.

[64] N. Thoti and Y. Li, “Design of GAA Nanosheet Ferroelectric Area Tunneling FET and Its Significance with DC/RF Characteristics Including Linearity Analyses,” *Nanoscale Research Letters*, vol. 17, no. 1, 2022.

[65] M. Kobayashi, K. Jang, N. Ueyama, and T. Hiramoto, “Negative Capacitance for Boosting Tunnel FET performance,” *IEEE Transactions on Nanotechnology*, vol. 16, no. 2, pp. 253–258, 2017.

[66] S. Singh, S. Singh, and A. Naughariya, “Negative Capacitance Dual Electrode Junctionless TFET Based on Si Doped HfO2 Ferroelectric Layer: Proposal and Optimization,” *Integrated Ferroelectrics*, vol. 221, no. 1, pp. 88–99, 2021.

[67] A. Rassekh, J.-M. Sallese, F. Jazaeri, M. Fathipour, and A. M. Ionescu, “Negative Capacitance Double-Gate Junctionless FETs: A Charge-Based Modeling Investigation of Swing, Overdrive and Short Channel Effect,” *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 939–947, 2020.

[68] Y. Choi, Y. Hong, and C. Shin, “Device design guideline for junctionless gate-all-around nanowire negative-capacitance FET with HfO2-based ferroelectric gate stack,” *Semiconductor Science and Technology*, vol. 35, no. 1, p. 015011, 2019.

[69] H. Mehta and H. Kaur, “Modeling and simulation study of novel Double Gate Ferroelectric Junctionless (DGFJL) transistor,” *Superlattices and Microstructures*, vol. 97, pp. 536–547, 2016.

[70] M. Rapp, S. Salamin, H. Amrouch, G. Pahwa, Y. Chauhan, and J. Henkel, “Performance, Power and Cooling Trade-Offs with NCFET-based Many-Cores,” *in Proc. 56th ACM/IEEE Design Automation Conference (DAC)*, 2019, pp. 1-6.

[71] S. K. Samal, S. Khandelwal, A. I. Khan, S. Salahuddin, C. Hu, and S. K. Lim, “Full chip power benefits with negative capacitance FETs,” *in Proc. IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, 2017, pp. 1-6.

[72] Y.-K. Lin, H. Agarwal, M.-Y. Kao, J. Zhou, Y.-H. Liao, A. Dasgupta, P. Kushwaha, S. Salahuddin, and C. Hu, “Spacer Engineering in Negative Capacitance FinFETs,” *IEEE Electron Device Letters*, vol. 40, no. 6, pp. 1009– 1012, 2019.

[73] S. Kaushal, S. Kaundal, and A. K. Rana, “Impact of Spacer Configuration on Negative Capacitance Multi Gate Junctionless FET,”

2021 International Conference on Computer Communication and Informatics (ICCCI), 2021.

[74] A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Gate-Induced Drain Leakage in Negative Capacitance FinFETs," *IEEE Transactions on Electron Devices*, vol. 67, no. 3, pp. 802-809, 2020.

[75] A. D. Gaidhane, G. Pahwa, A. Dasgupta, A. Verma, and Y. S. Chauhan, "Compact Modeling of Surface Potential, Drain Current and Terminal Charges in Negative Capacitance Nanosheet FET including Quasi-Ballistic Transport," *IEEE Journal of Electron Devices Society*, vol. 8, pp. 1168-1176, 2020.

[76] F. Bellando, C. K. Dabhi, A. Saeidi, C. Gastaldi, Y. S. Chauhan, and A. M. Ionescu, "Subthermionic negative capacitance ion sensitive field-effect transistor," *Applied Physics Letters*, vol. 116, no. 17, p. 173503, 2020.

[77] S. Salamin, G. Zervakis, F. Klemme, H. Kattan, Y. Chauhan, J. Henkel, and H. Amrouch, "Impact of NCFET Technology on Eliminating the Cooling Cost and Boosting the Efficiency of Google TPU," *IEEE Transactions on Computers*, vol. 71, no. 4, pp. 906–918, 2022.

[78] B. Awadhiya, S. Yadav, P. Upadhyay, and P. N. Kondekar, "Effect of back gate biasing in negative capacitance field effect transistor," *Micro and Nanostructures*, vol. 166, p. 207226, 2022.

[79] T. Kim and C. Shin, "Effects of Interface Trap on Transient Negative Capacitance Effect: Phase Field Model," *Electronics*, vol. 9, no. 12, p. 2141, 2020.

[80] C. Jiang, L. Zhong, and L. Xie, "Impact of Interface Trap Charges on the Electrical Characteristics of Back-Gated 2D Negative Capacitance (NC) FET," *IEEE Transactions on Nanotechnology*, vol. 18, pp. 1204–1207, 2019.

[81] A. Gupta, G. Bajpai, P. Singhal, N. Bagga, O. Prakash, S. Banchhor, H. Amrouch, and N. Chauhan, "Traps Based Reliability Barrier on Performance and Revealing Early Ageing in Negative Capacitance

FET,” *2021 IEEE International Reliability Physics Symposium (IRPS)*, 2021.

[82] H.-P. Lee, K.-Y. Tseng, and P. Su, “Interface discrete trap induced variability for negative capacitance FinFETs,” *2018 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)*, 2018.

[83] H. Amrouch, G. Pahwa, A. D. Gaidhane, C. K. Dabhi, F. Klemme, O. Prakash, and Y. S. Chauhan, “Impact of Variability on Processor Performance in Negative Capacitance FinFET Technology,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 9, pp. 3127–3137, 2020.

[84] T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, “Impact of Process Variations on Negative Capacitance FinFET Devices and Circuits,” *IEEE Electron Device Letters*, vol. 39, no. 1, pp. 147-150, 2018.

[85] C. Lin, A. I. Khan, S. Salahuddin, and C. Hu, “Effects of the Variation of Ferroelectric Properties on Negative Capacitance FET Characteristics,” *IEEE Transactions on Electron Devices*, vol. 63, no. 5, pp. 2197-2199, 2016.

[86] T. Dutta, V. Georgiev, and A. Asenov, “Stability and Vmin analysis of ferroelectric negative capacitance FinFET based SRAM in the presence of variability,” *Solid-State Electronics*, vol. 184, p. 108100, 2021.

[87] C. Wang, J. Wu, H. Yu, G. Han, X. Miao, and X. Wang, “Effects of Temperature on the Performance of $Hf_{0.5}Zr_{0.5}O_2$-Based Negative Capacitance FETs,” *IEEE Electron Device Letters*, vol. 41, no. 11, pp. 1625–1628, 2020.

[88] J. Jo and C. Shin, “Impact of temperature on negative capacitance field-effect transistor,” *Electronics Letters*, vol. 51, no. 1, pp. 106–108, 2015.

[89] O. Prakash, G. Pahwa, C. K. Dabhi, Y. S. Chauhan, and H. Amrouch, “Impact of Self-Heating on Negative-Capacitance FinFET: Device-

Circuit Interaction," *IEEE Transactions on Electron Devices*, vol. 68, no. 4, pp. 1420– 1424, 2021.

[90] D. Jimenez, E. Miranda, and A. Godoy, "Analytic Model for the Surface Potential and Drain Current in Negative Capacitance Field-Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 57, no. 10, pp. 2405–2409, 2010.

[91] C. Jiang, R. Liang, J. Wang, and J. Xu, "Analytical drain current model for long-channel gate-all-around negative capacitance transistors with a metal– ferroelectric–insulator–semiconductor structure," *Japanese Journal of Applied Physics*, vol. 55, no. 2, p. 024201, 2016.

[92] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Compact Model for Ferroelectric Negative Capacitance Transistor With MFIS Structure," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 1366–1374, 2017.

[93] A. D. Gaidhane, G. Pahwa, A. Verma, and Y. S. Chauhan, "Compact Modeling of Drain Current, Charges, and Capacitances in Long-Channel Gate-All-Around Negative Capacitance MFIS Transistor," *IEEE Transactions on Electron Devices*, vol. 65, no. 5, pp. 2024–2032, 2018.

[94] R. Liang, C. Jiang, J. Wang, J. Xu, and T. Ren, "An analytical charge-sheet drain current model for monolayer transition metal dichalcogenide negative capacitance field-effect transistors," *in Proc. IEEE Electron Devices Technology and Manufacturing Conference (EDTM)*, 2017, pp. 268-269.

[95] C. K. Dabhi, S. S. Parihar, A. Dasgupta, and Y. S. Chauhan, "Compact Modeling of Negative-Capacitance FDSOI FETs for Circuit Simulations," *IEEE Transactions on Electron Devices*, vol. 67, no. 7, pp. 2710-2716, 2020.

[96] H. Eslahi, T. J. Hamilton, and S. Khandelwal, "Small signal model and analog performance analysis of negative capacitance FETs," *Solid-State Electronics*, vol. 186, p. 108161, 2021.

[97] N. Pandey and Y. S. Chauhan, "Analytical Modeling of Short-Channel Effects in MFIS Negative-Capacitance FET Including Quantum

Confinement Effects," *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 4757– 4764, 2020.

[98] Y. Dong, R. Han, D. Wang, R. Wang, and C. Guo, "An analytical model including interface traps and temperature effects in negative capacitance double gate field effect transistor," *Silicon*, vol. 13, no. 9, pp. 3101–3111, 2020.

[99] Y.-K. Lin, H. Agarwal, P. Kushwaha, M.-Y. Kao, Y.-H. Liao, K. Chatterjee, S. Salahuddin, and C. Hu, "Analysis and modeling of inner fringing field effect on negative capacitance FinFETs," *IEEE Transactions on Electron Devices*, vol. 66, no. 4, pp. 2023–2027, 2019.

[100] S. Kaushal and A. K. Rana, "Analytical modelling and simulation of negative capacitance junctionless FinFET considering fringing field effects," *Superlattices and Microstructures*, vol. 155, p. 106929, 2021.

[101] S. Kaushal and A. K. Rana, "Analytical model of subthreshold drain current for nanoscale negative capacitance junctionless FinFET," *Microelectronics Journal*, vol. 121, p. 105382, 2022.

[102] S. Kaushal and A. K. Rana, "Modelling and Analysis of Gate Induced Drain Leakage Current in Negative Capacitance Junctionless FinFET," *Journal of Computational Electronics*, 2022.

Note

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11
Application of Ferroelectrics: Monolithic-3D Inference Engine with IGZO Based Ferroelectric Thin Film Transistor Synapses

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Abstract

Instigated by the plethora of data generated by edge devices and IoT devices, machine learning has become the *de facto* choice of everyone for solving many tasks. Applications such as intelligent healthcare monitoring systems, smart watches, or automatic cars require real-time processing of data and images, which is done by machine learning algorithms with higher efficiency than humans. There are two possible methods for artificial intelligence:

1. Non-von-Neumann hardware-based implementation of neural networks
2. Traditional computer science-based approach for neural networks or traditional von-Neumann architecture-based implementation of neural networks

The standard von-Neumann performance of neural networks, where the memory and computation parts are segregated, suffers from severe latency with an increasing number of edge devices. However, the multitude of edge devices used in our daily life imposes strict restrictions on latency, device area, and power consumption for hardware. Therefore, we need to take the

route beyond the CMOS-based mixed-signal implementation of neural networks where the memory bandwidth is not limited by the quintessential von-Neumann architecture. The primary motivation of present-day research on the non-von-Neumann computing architecture is to build dedicated hardware modules for implementing low-power, fast-computing units without affecting the recent trend of scaling.

This chapter focuses on amorphous indium-gallium-zinc-oxide (α-IGZO) based devices and their system-level applications. Back-end-of-line (BEoL) compatible indium IGZO based multibit one-time programmable (OTP) ferroelectric thin film transistors (FeTFT) with lifelong retention capability were fabricated. The maximum temperature of the entire fabrication process was limited to 350°C. The gate-stack engineering by varying the thickness ratio of ferroelectric hafnium zirconium oxide (HZO) and IGZO layer fomented excellent data-retention capability and one-time programming properties. Further, we have evaluated the performance of IGZO-based FeTFT as synaptic devices for an inference engine. The system-level simulation revealed inference accuracy loss of only 1.5% after ten years without re-training for the Modified National Institute of Standards and Technology (MNIST) hand-written digits in a multi-layer perceptron (MLP) neural network with a baseline of 97%. The proposed inference engine also showed superior energy efficiency and a cell area of 95.33 TOPS/W (binary) and $8F^2$, respectively.

***Keywords*:** Ferroelectric Fin FET, $Hf_{0.5}Zr_{0.5}O_2$, random variations, systematic variations, junction temperature variations, neural networks, neuromorphic computing

11.1 Introduction

From the earliest time of civilization, humans dreamed of creating machines that they could have complete control over, yet worked on their own . *Greek* mythological tales tell the story of such machines. As human beings became more intelligent over time and intelligence was inherited from our ancestors, we stepped closer to creating such machines. The ***Antikythera Mechanism*** from ancient *Greek* civilization, used to predict astronomical events in advance [1], is the first known computer in human history. According to the Oxford dictionary, the word *"Computer"* was used as a

job title to describe people who used to perform calculations in the early 1600s, which was later changed to describe calculating machines when **Charles Babbage**, the father of the computer, first designed the difference engine in the 19^{th} century. However, this whole paradigm of **"Computer"** was changed by **Alan Turing**, the inventor of *"Computer Science"*, in 1936. Since then, the world has watched the evolution of computers and computer science.

Today's computer scientists focus on making computers more intelligent by developing ***Artificial Intelligence***. The root of ***Artificial Intelligence*** lies in the fact that machines can learn in a systematic way, where we reiterate the assigned work to optimize machine parameters. The biggest challenge in artificial intelligence (AI) lies in the type of problem. Problems that can be described with mathematical formalism may seem difficult for a human being but are pretty straightforward for the computer. In contrast, problems which are difficult to express by mathematical formalism become difficult for the computer to solve. Therefore, a computer seems to be a better chess player than a human being, but finds it very difficult to recognize speech or images, which is intuitively done by us [2]. Therefore, the biggest catch in present-day artificial intelligence lies in teaching the computer how to perform a task that cannot be represented by mathematical formalism. Several researchers [3] attempted hard-coding techniques to infuse informal knowledge into the computer, recognized as the knowledge-based approach to artificial intelligence. However, none of this research is widely accepted due to the cumbersome coding process and complexity of expressing the informal worldly knowledge into typical mathematical formalism.

The difficult part of hard-coding parts for the real world into a computer necessitated the self-learning feature in machines, called *machine learning*. The advent of machine learning instilled decision-making capability in computers. Many complex tasks like separating legit e-mails from spam can be accomplished by using a simple machine learning algorithm. The performance of such *machine learning* algorithms is dependent on the representation of the dataset they are provided with, which is very much common in our daily lives. However, a problem like extracting feature values from photographs under different environmental conditions makes the task complicated. The solution to this kind of problem uses *representation learning* and *deep learning* [2]. Deep learning builds

complex concepts with simpler concepts as the base. A fundamental feature is taken as the basic building block for a very complicated task.

The goal of an MLP network is to learn the best approximate value of a parameter, known as synaptic weight, through iterative training. x_{ij} in Figure 11.1 represents the input to the system and the network maps the input x through the activation function f for obtaining some output value y_{ij}. The mapping relation can be written as $y_{ij} = f(x_{ij}, w_{ij})$. The key task of the network is to learn the value of w_{ij}.

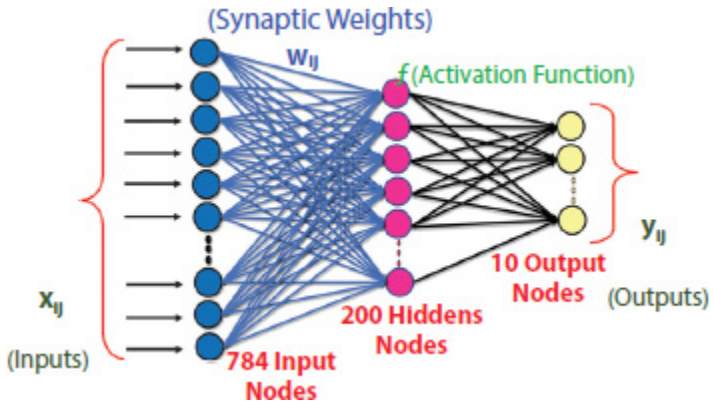

Figure 11.1 Schematic representation of a multi-layer perceptron neural network consisting of 784 input nodes, 10 output nodes, and 200 hidden nodes in one hidden layer between the input and the output layer.

When an MLP network receives an input x_{ij} to map it to the output y_{ij}, information flows through the network in a forward direction. This method is called *forward propagation*. During training, *forward propagation* continues until the network generates a cost function, $J(w_{ij})$, which is sent backwards throughout the network via a *back-propagation* algorithm [4] for computing the gradient. The term *back-propagation* only refers to the calculation of gradient, which is otherwise computationally expensive. The convolutional neural network (CNN) architecture is shown in Figure 11.2, where several convolution and pooling functions are inserted in front of the fully connected MLP part. Convolution uses several filters, called kernels, to extract the features and the pooling function is used to compress the extracted feature to minimize the pixels to be dealt with. After layers of feature extraction, the data will go to the fully connected MLP section to classify the input and determine the final prediction result. The training

method of CNN is similar to the MLP. It uses gradient descent and back-propagation as the main training algorithm. With the help of convolution and pooling, we can detect the input's feature and the target position problem can be fixed. On the other hand, once the input can be transferred into the image-like form, it is suitable for CNN training. Moreover, since the size of kernels is quite small, it usually needs only one fully connected layer as a classifier. It can relieve the tremendous need for memory capacity.

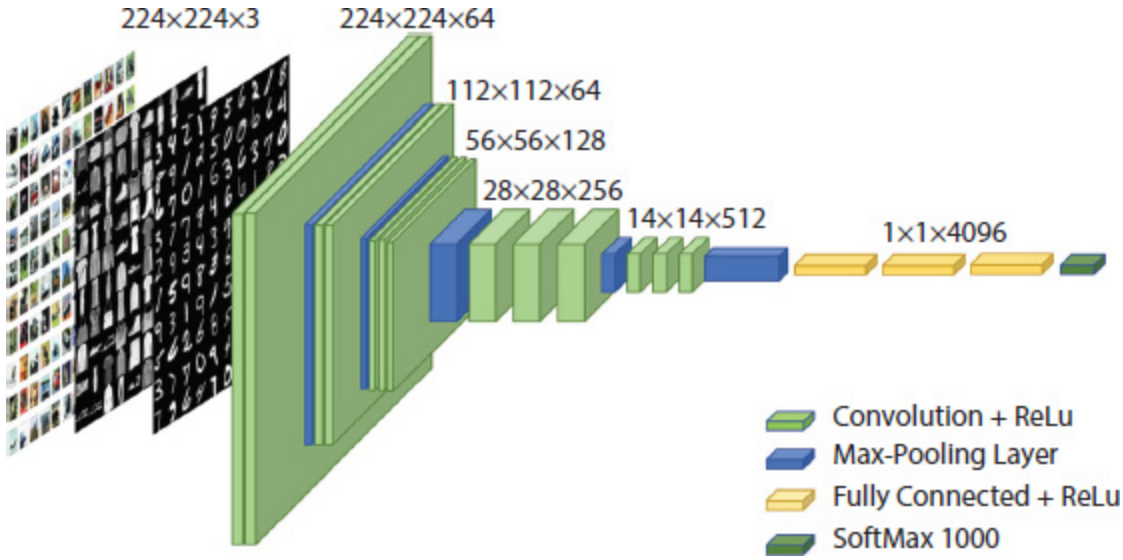

Figure 11.2 Schematic representation of VGG-16 convolutional neural network.

In the last ten years, the world has seen progress in the research of neural networks (Figure 11.3). The advent of LeNET [5, 6] in recent times has made machine learning or neural network-based computation an inevitable choice for solving many complex tasks. Nevertheless, the artificial neural networks (ANN) implemented in traditional *von-Neumann* computing systems endure severe bottlenecks during the data transfer between segregated memory units and processing units. Therefore, this computer science-based approach of [7, 8] artificial neural networks (ANN) in these data centers fail to imitate true brain functions in terms of power consumption and speed of operations. Therefore, researchers showed interest in building hardware-based neural networks along with software counterparts. The period between the late 1980s to early 1990s saw the advent of first-generation neuromorphic chips [9–12]. Later on, the

scientific community understood that the first-generation neural network could not match the performance of Boolean computing of digital computers due to difficulties in integrating synapses and neurons at the hardware level. Therefore, neuromorphic computing took a back seat, while conventional computers exploiting the scaling of CMOS technology moved forward by leaps and bounds. In recent years, as we progress towards Moore's law and breakthroughs in the research of deep learning, research interests in hardware implementation of neural networks have been reinvigorated. Therefore, notable interest in the area of emerging non-volatile memory based non-von-Neumann computing-oriented implementation of lowpower neural networks [13–22] has grown and the arrivals of Loihi chip from Intel [23] and TrueNorth [24] from IBM rang the bell for next-generation computing architecture. Amidst many developments, research on the feasibility of implementing neural networks on hardware and the quest for finding a perfect synaptic device is still on.

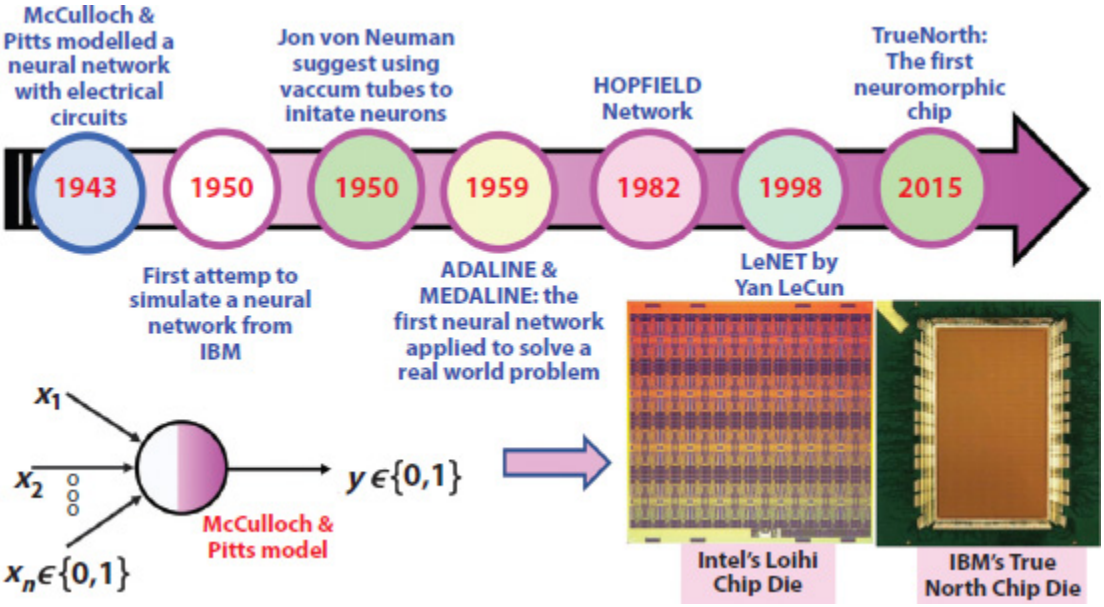

Figure 11.3 Historical timeline and major milestones in research of neural networks and neuromorphic computing.

The last few decades have seen the evolution of edge electronic devices like the smartwatch, smartphone, and others. This evolution had two trends. Primarily, the devices became smaller and cheaper, driven by ***Moore's Law,*** and the amount of information processed by these devices increased exponentially. Present-day edge devices like wearable devices and

smartphones use different types of sensors for performing different tasks. The data originating from all these sensors needs to be processed as well. This tendency necessitates the implementation of data-centric computing rather than rule-based computing. Apart from this, the plethora of data in the edge devices creates an opportunity to build a cloud-based platform for added intelligence to process the data more wisely. Deep learning comes to the rescue here. Machine learning or deep learning has emerged as a powerful choice for solving many complicated tasks in recent times. Despite the favorable results in small-scale applications, the real-life application of a deep neural network requires billions of synapses to be designed in the system. The training process for such a vast neural network requires a long time and tremendous energy, even when dedicated graphics processing units (GPUs) are deployed along with largely parallelized matrix solvers. Soon, the number of edge devices, especially wearable monitoring devices, cellphones, and other edge devices will explode. Power consumption is one of the most important aspects to be considered for all these applications. Neither implementing deconvolutional neural networks (DNN) in power-hungry GPUs nor directly uploading raw data to cloud computing for further analysis is viable. To overcome this issue, the long toil from both industry and academia has built ultra-low-power DNN accelerators. Google's tensor processing unit (TPU), to accelerate deep-learning applications in their data center, is a stark example [25]. Microsoft has exploited intelligent systems based on field-programmable gate arrays (FPGAs) in their data centers as well [26]. Further, the invention of *Intel*'s AI processor *"Nervana"* aims to revolutionize AI computing across many different fields. Apart from the great efforts and interest from the industry, academia has also spent significant time and effort in recent years to investigate various neural network architectures and hardware-based design topologies for building energy-efficient ANN accelerators.

11.2 Ferroelectricity in Hafnium Oxide

For the implementation of hardware-based neural network accelerators, specialized embedded non-volatile memory devices are required. One promising group is devices based on ferroelectric hafnium (zirconium) oxide. The ferroelectric phase in hafnium oxide, which was discovered in 2008 [27, 28], differs strongly from other common ferroelectrics, like

barium titanate (BTO) or lead titanate zirconate (PZT), due to its different crystallographic symmetries. While common ferroelectric materials are of perovskite structure, hafnium oxide and zirconium oxide-based ferroelectrics exhibit a fluorite structure, namely an orthorhombic phase with the space group $Pca2_1$ [29]. The CMOS compatibility and the low process temperature of hafnium zirconium oxide (HZO) make HZO-based ferroelectric (Fe) finFETs an excellent candidate for logic, memory, and neuromorphic devices. This property can be attributed to its superior endurance and write speed compared to flash, significantly higher on-tooff current ratio over that of MRAM, and the negligible impact of random telegraphic noise from charge-based operation, unlike RRAM [30–37]. However, the pivotal issue lies in the increasing stochasticity with scaling and the inherent charge-trapping sites that can capture electrons or holes from the channel side (CS) or the gate side (GS). These effects create serious reliability problems in terms of endurance degradation and increased variation during program–erase (WRITE) operation in deep-scaled HZO-based ferroelectric FET (Fe-FET) devices. There have been numerous efforts from the scientific community to find possible solutions to mitigate these nonidealities for improving the performance of ferroelectric FETs. However, previous studies on Fe-FET variability have focused mainly on large (>1 μ^2) and planar MOSFET devices in which the random distribution of ferroelectric–dielectric domains and trapping are the two primary sources of variation.

The following sections will therefore provide an overview of the thermodynamics, kinetics, domain dynamics, and microstructure of this material system and how these affect the local variability in the ferroelectric layer.

11.2.1 Thermodynamic and Kinetic Origin of the Ferroelectric Phase

Besides the ferroelectric $Pca2_1$ phase (see Figure 11.4a), other phases are thermodynamically (meta) stable. Density functional theory (DFT) calculations have revealed that the thermodynamical ground state is formed by the monoclinic phase with space group $P\ 2_1/c$ [38]. Moreover, other phases like the tetragonal $P\ 4_2/nmc$, cubic $Fm\bar{3}m$, and orthorhombic *Pcba*

phase (Figure 11.4) have been found at similar energy values to the ferroelectric phase [38, 39]. This has multiple implications: i) the ferroelectric $Pca2_1$ phase is metastable, meaning that the phase has to be stabilized kinetically or by means of, e.g., doping; ii) the multitude of phases might manifest itself via polymorphism and co-existing phases in polycrystalline films; iii) the film might undergo phase transitions when applying temperature, mechanical, or electrical stress.

The kinetic stabilization of the ferroelectric phase has been described in the literature as well [41]. The material first nucleates in a high symmetry phase, most likely the tetragonal phase. Upon heating, these nuclei grow and a fully crystalline film is formed. Upon cooldown, the phase transition temperature to the monoclinic phase is reached. This transition requires shearing of the crystallographic planes [28] and can be kinetically suppressed, e.g., by the presence of a capping layer [28] or fast cooling [42]. Further reduction in temperature leads to the Curie temperature, where the tetragonal phase transitions to the orthorhombic phase. If the monoclinic phase transition was suppressed, the resulting film consists predominantly of the ferroelectric phase.

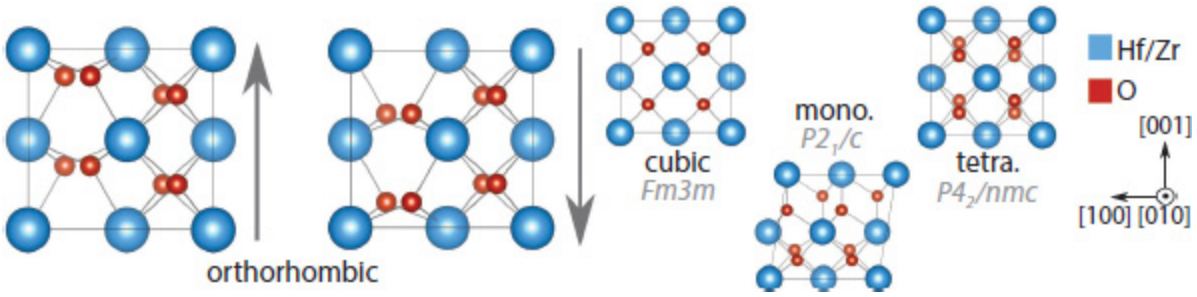

Figure 11.4 Crystallographic phases and their unit-cells in Quasi-cubic representation. All Figures reproduced with permission from [40].

A wide variety of dopants have already been confirmed to stabilize the $Pca2_1$ phase, with the most notable doping elements being Si, La, Al, Y, and Hf/Zr for ZrO_2/HfO_2, respectively [28, 43–46]. It was furthermore found that the doping profiles can be normalized, thus showing a universal profile [47]. Here, low doping levels result in a monoclinic phase, whereas high levels result in a tetragonal or even cubic phase [48, 49]. Moreover, close to the phase boundary towards the tetragonal phase, antiferroelectric-like behavior can be observed [28, 49]. Electrical field cycling, however,

often results in a transition back to ferroelectric behavior. This effect is known as classical wake-up and a detailed discussion on this phenomenon can be found elsewhere [50].

Even though doping is usually used to stabilize the ferroelectric phase, it can even be stabilized in undoped hafnium oxide layers as shown in Figure 11.5 [51]. Here, a strong dependence on the film thickness can be observed [51], most likely related to the residual mechanical stress due to thermal expansion mismatch [52]. Other works have highlighted the importance of mechanical stress on phase stabilization as well [53–55]. It has even been shown that the optimal doping concentration shifts depending on the residual mechanical stress [56]. Consequently, the phase diagram of hafnium/zirconium oxide can be described in terms of mechanical stress, as shown in Figure 11.6. Therefore, the control of mechanical stress is of major importance for the device performance and local variability will be reflected in the device variability.

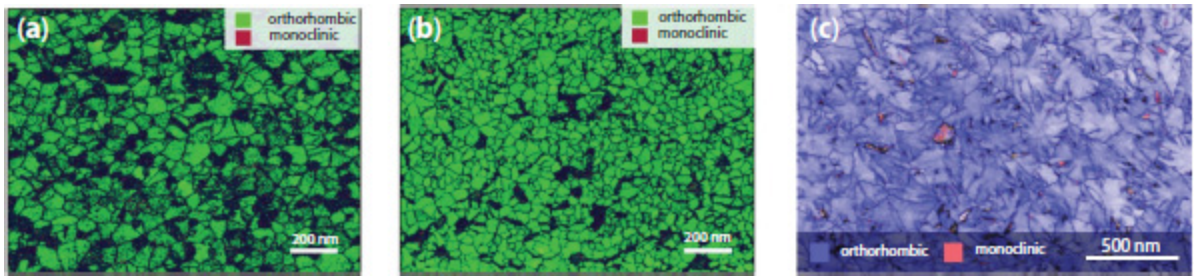

Figure 11.5 Transmission Kikuchi Diffraction (TKD) phase map images of Si- and Zr-doped HfO_2 Films. a) and b) show the microstructure of Si:HfO_2 and $Hf_{0.5}Zr_{0.5}O_2$ thin films grown on TiN. The microstructure of a Si:HfO_2 film grown on SiO_2 is shown in c). All Figures are reproduced with permission from: a), b) [66], and c) [65].

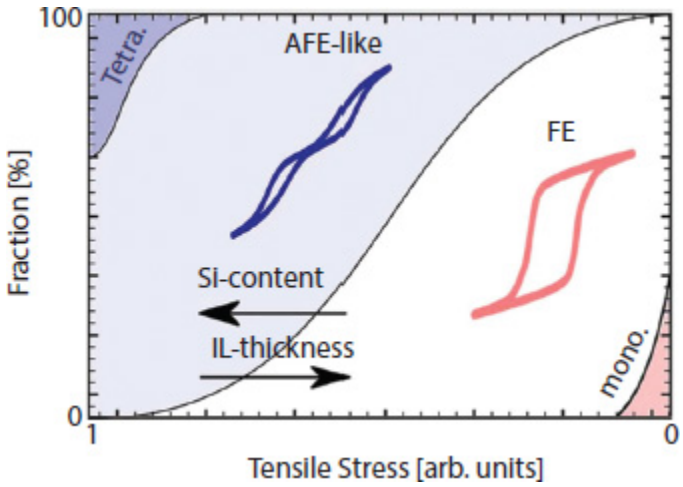

Figure 11.6 Schematic representation of stress dependence of Hafnium oxide. Figure reproduced with permission from [56].

11.2.2 Microstructure-Based Variability in Ferroelectric Response

Another source of device variability is the microstructure of the film [57–61]. This includes the grain structure, local crystallographic phase, and local crystallographic orientation. The introduction of transmission Kikuchi diffraction as a viable method to study hafnium oxide enabled a detailed study of these parameters [62]. As expected from the discussion on thermodynamics, the number of monoclinic grains increases for low doping concentrations [63]. Moreover, the monoclinic phase fraction increases when the annealing temperatures are in the range of or higher than 1000°C [64, 65].

In addition to differences in the monoclinic phase fraction, grain size and crystallographic texture are influenced by changes in the process conditions. First of all, it has been shown that different dopants result in different grain sizes [63, 66], for example, Si exhibits much larger grains compared to HZO (Figure 11.5 [66]). Additionally, it has been shown that in the range of 750°C to 950°C a semi-epitaxial growth of Si:HfO_2 can be observed, resulting in polarization hysteresis with high remanent polarization and square-like behavior [52]. Another major influence is the sub-strate. While strong crystallographic textures with <100> orientation are observed on pre-textured TiN substrate [52, 66], layers grown on SiO_2 show only weak textures with <111> or <110> orientation [52, 65].

Moreover, the grain size is much larger with approximately 230 nm [65], compared to samples grown on TiN, which show an average of 10 nm to 50 nm [66]. Furthermore, these large grains show a dendritic structure (Figure 11.5c), in stark contrast to the previously observed disc-shaped grains [52].

These differences in microstructure indeed affect the device variability, which has been confirmed by studying the influence of the device dimensions, namely channel width and length [57]. The observed trends in the switching behavior and variability nicely match the expected behavior when considering the presence of current percolation paths [57]. It has furthermore been shown that changes in the crystallographic texture and grain size strongly alter the switching behavior [67, 68]. Moreover, an impact on device variability due to grain statistics has been confirmed as well [58–60, 69].

11.3 IGZO Based Ferroelectric Thin Film Transistor

One promising embedded non-volatile memory based on ferroelectric hafnium oxide is the ferroelectric thin film transistor (FeTFT). Since it can be integrated into the back-end-of-line (BEoL) using hafnium zirconium oxide (HZO), the integration into integrated circuits will differ strongly from the front-end-of-line (FEoL). Nevertheless, these devices were only recently first demonstrated.

11.3.1 Integration and Performance of FeTFT Devices

On a basic level, the performance of ferroelectric hafnium oxide in conjunction with oxide semiconductors was first evaluated by comparing the performance of metal-ferroelectric-metal (MFM) and metal-semiconductor-ferroelectric-metal (MSFM) capacitors. These were prepared on highly-boron doped 300 mm silicon wafers using CMOS compatible industry standard production tools, as presented in [70]. The titanium nitride (TiN) based bottom electrode was deposited via atomic layer deposition (ALD). The ferroelectric HZO layer was deposited via ALD at 300°C. Hafnium tetrachloride ($HfCl_4$), zirconium tetrachloride ($ZrCl_4$), and water (H_2O) were used as the precursors and oxidizer,

respectively. The thickness of the films was adjusted by the number of total deposition cycles. The thickness varied between 5 and 20 nm. In the case of the MSFM capacitors, the IGZO was deposited by radio frequency magnetron sputtering from a ceramic target (In:Ga:Zn=1:1:1) with an argon to oxygen ratio of 33.3:1 and a pressure of 1 µbar. The thickness of the IGZO semiconductor varied between 5 and 30 nm. An interfacial layer (IL) of 2 nm of aluminum oxide (Al_2O_3) was deposited by ALD using trimethyl aluminum and H_2O. The TiN top electrode was deposited by magnetron sputtering at temperatures below 100°C to avoid *in-situ* crystallization of the HZO films. The thermal annealing for crystallization was carried out at 350°C in a nitrogen atmosphere within a furnace-type oven for one hour. The resulting MFM and MFIS devices therefore allow a direct comparison of the performance of the ferroelectric layer. An in-depth discussion on this topic can be found in [70]. One major finding was that the thickness of the oxide semiconductor is of major importance due to the more than significant difference in majority and minority charge carrier mobility. In the case of IGZO, the hole mobility is approximately zero [70]. Nevertheless, using oxide semiconductors offers a major advantage to those that are Si-based due to free choice of material or even absence of the interface layer [71–74].

Recently, multiple groups have demonstrated hafnium oxide-based FeTFT devices [70, 72, 74–76]. Here, a large range of applications has been addressed, ranging from 2D- and 3D-NAND architectures [73, 74] to display calibration devices [70]. In addition, these devices have been proposed as a viable candidate for neuromorphic applications [70, 72, 77]. The researchers fabricated the FeTFTs on silicon wafers with an insulating layer of 100 nm silicon dioxide (SiO_2). 50 nm of TiN bottom gate was deposited by ALD. The bottom gate patterning was done via e-beam lithography and reactive ion etching. A 10 nm thick HZO based ferroelectric layer was deposited by ALD and it was followed by deposition of 2 nm Al_2O_3. The IGZO channel layer of desired thickness was deposited by magnetron sputtering. The contacts for source and drain consisting of titanium-aluminum-titanium (Ti/Al/Ti) were deposited by electron-beam evaporation and patterned by a lift-off technique. The opening of contacts to the bottom gate was achieved by using a dry etching process. Finally, the

devices were annealed at a temperature of 350°C for a duration of one hour [70]. An overview of the process flow is provided in Figure 11.7.

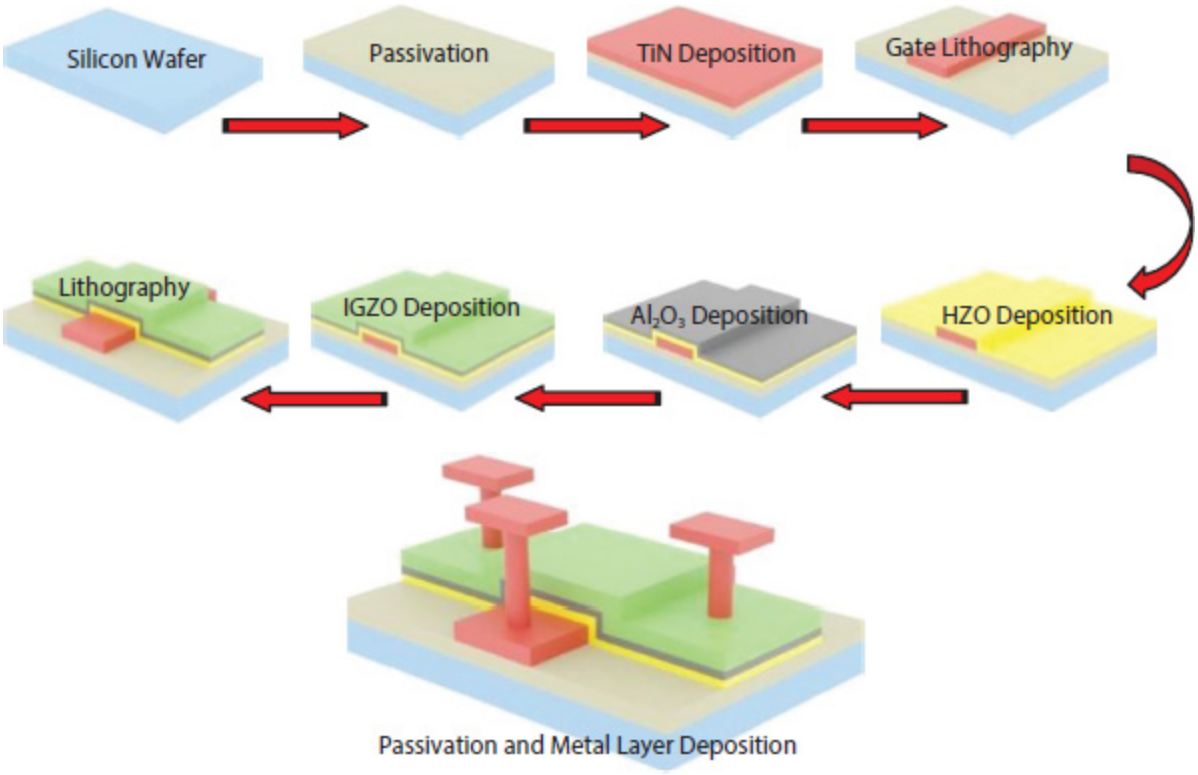

Figure 11.7 Process flow for fabricating IGZO-based FeTFT.

11.3.2 Characterization of FeTFT-Based Neuromorphic Devices

In order to evaluate the performance of FeTFTs for hardware-based neural network accelerators, the synaptic performance was investigated. The transfer characteristics of exemplary FeTFT devices [70] for different polarization states clearly indicate that two-bit operation (8 V_{th} states) is feasible, as demonstrated in Figure 11.8. One option is the programming of the device through an amplitude increasing of a gate positioned single pulse 8a and a second option is for the gate pulse to increase the pulse width 8b. Both options can be used and combined. While setting the single pulse on the gate contact, the drain and source contact is set at the ground potential. After switching to programmed states (increasing the pulse amplitude), the V_{th} shifts to negative values based on a change of polarization in the ferroelectric layer. The same effect is also possible for a change in the pulse width or a combined version of programming. The switching effect has a

maximum at full polarization of the ferroelectric layer and these states and the states in between can be switched to with very high accuracy [70]. Similar results have also been reported by M.-K. Kim *et al.*, which furthermore confirmed excellent linearity and symmetry in the conductance change [72, 77]. Nevertheless, the device-to-device variation in smaller geometric devices is influenced by the aforementioned microstructural sources, as well as by low frequency noise.

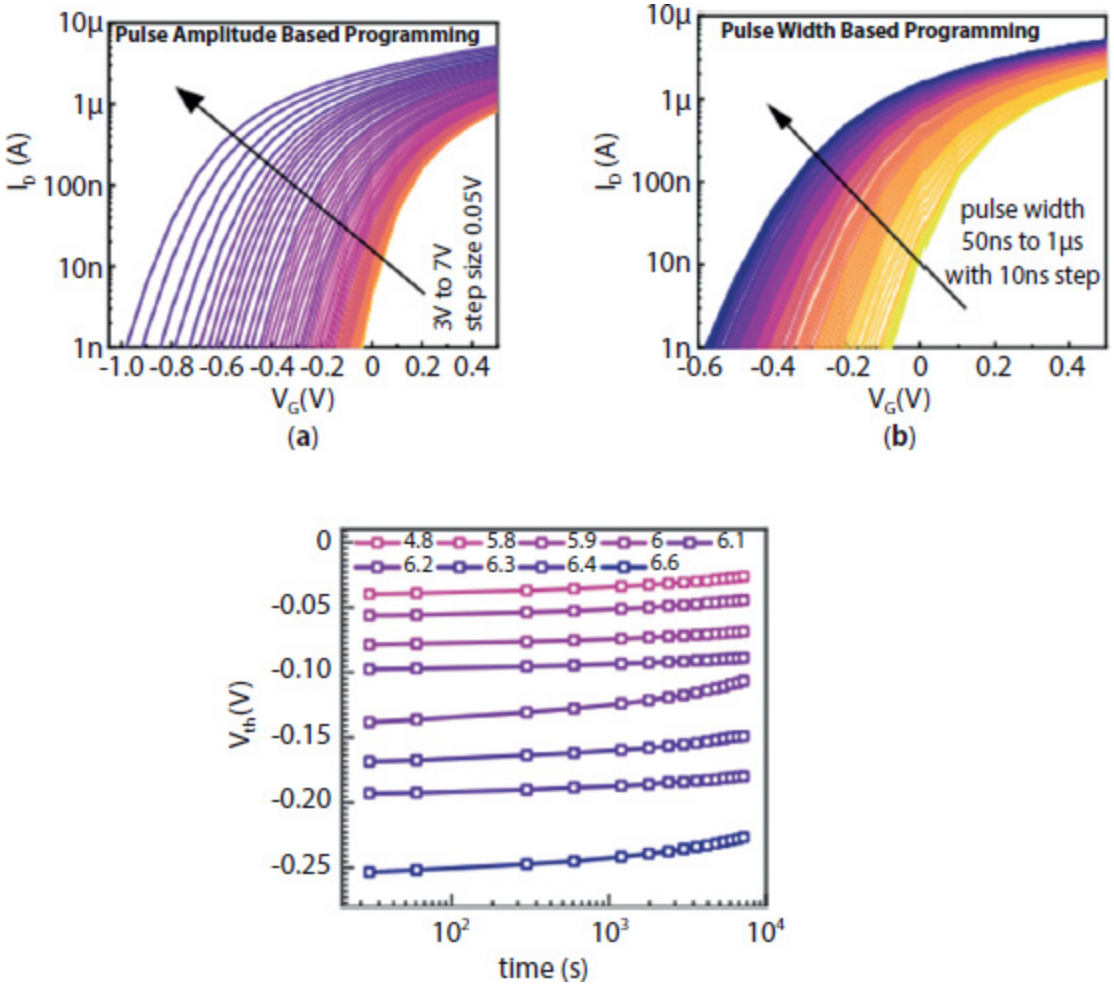

Figure 11.8 Transfer Characteristics of FeTFTs with 30 nm IGZO. Partial switching of the ferroelectric stack was conducted by applying voltage pulses to the gate. (a) The amplitude was varied from 3 V to 7 V, keeping the width of the pulse fixed at 200 ns. (b) The width was varied between 50 nm and 1 µs and the amplitude was fixed at 5.5 V.

This low frequency noise influence is difficult to investigate for single states since the state can switch during the measurement due to disturbance.

The method to measure low frequency noise of a stable state is demonstrated elsewhere [78]. The difference between this V_{th} minimum and maximum shows a memory window of about 1 V during the pulsing with amplitude variation (0.5 V steps) or with pulse width variation. The field effect mobility (μ_{eff}) (detailed investigation in [70]) and the sub-threshold slope ($S_{th}S$) show a low decline, as presented in Figure 11.8. Pulse amplitude change-based switching the μ_{eff} shows a decline of (+3.4%), while in the programming method with a change only in the pulse width, the mobility changed by 19%. For $S_{th}S$, in the case of pulse amplitude increase, a change from 65.3 $\frac{mV}{dec}$ to 103 $\frac{mV}{dec}$ is observed. On the other hand, the

$S_{th}S$ changes only slightly in the case of the second method. These changes in both cases can be based on interface defects and occur especially after a high number of cycles. An in-depth analysis and detailed understanding of the defect behavior of the ferroelectric layer and the interface can be found elsewhere [79]. Summarized, it is a tradeoff between a better $S_{th}S$ or a better μ_{eff} performance that means avoiding mobility variations, as well as a significant change in the $S_{th}S$ as a combination of the pulse width and amplitude change in programming the devices. The retention of different states is demonstrated with a stable V_{th} during a time period of two hours in Figure 11.8c. An extrapolation up to ten years shows a decrease in polarization of around 20%.

11.4 Applications in Neural Networks

Neuromorphic simulations were performed to quantify the performance of FeTFT as synaptic devices. The program-erase characteristics, along with the experimentally obtained device variations in terms of standard deviations in drain current distribution have been used to train an FeTFT-based multilevel perceptron (MLP)–based neural network with the MNIST data set [80]. The training can be done using two scenarios. The first scenario is online training where the samples from the data set are directly

used to train the hardware-based neural network. For simulating the online training scenario, device-to-device variation is considered to be fixed throughout the training process and the cycle-to-cycle variation changes randomly during weight update and verification process. The second scenario is offline training. During offline training, the synaptic weight coefficients of the neural network are obtained by conducting training operations in software without considering realistic hardware-related variations. The weights are then updated in the hardware. Both of the training processes are followed by the inference operation which focuses on prediction. It has been noted in the literature that online training of the neural network requires high endurance devices and that it is power hungry in nature [30, 35]. Apart from this, recent works on ferroelectric memories have also focused on 3D-integration [77, 81, 82]. Therefore, we focus on the inference-only operation and monolithic-3D integration of ferroelectric memories.

11.4.1 Monolithic 3D Inference Engine

Finally, the system level validation of the monolithic-3D (M3D) inference engine was performed using the simulation platform described in [35, 83–87]. The *modus operandi* for IGZO based FeTFT M3D inference engines are described in Figure 11.9. We only consider inference-only operation on a multilevel perception-based neural network (MLP-NN) with offline training. The neural network was trained with the MNIST data set, saving the WRITE endurance limit of the FeFET devices. The MLP neural network has three layers. The input-layer consists of 784 nodes, the hidden layer has 200 nodes, and the output layer has ten nodes. The input image was divided onto 28 × 28 pixels which correspond to 784 nodes. Ten output nodes correspond to the ten digits of the MNIST data set. The neural network uses the sigmoid function as an activation function. The accuracy drop due to retention degradation was limited to only 1.5% over 10 years, while for other state-of-the-art Fe devices only an 11% inference accuracy remained. We have furthermore simulated the impact of analog-to-digital-converter (ADC) precision in the inference engine, which shows that using area-efficient 1-bit ADCs can boost the system performance in terms of area, energy efficiency with only an accuracy drop of 1.87%, and maintaining an inference accuracy above 94% for 10 years.

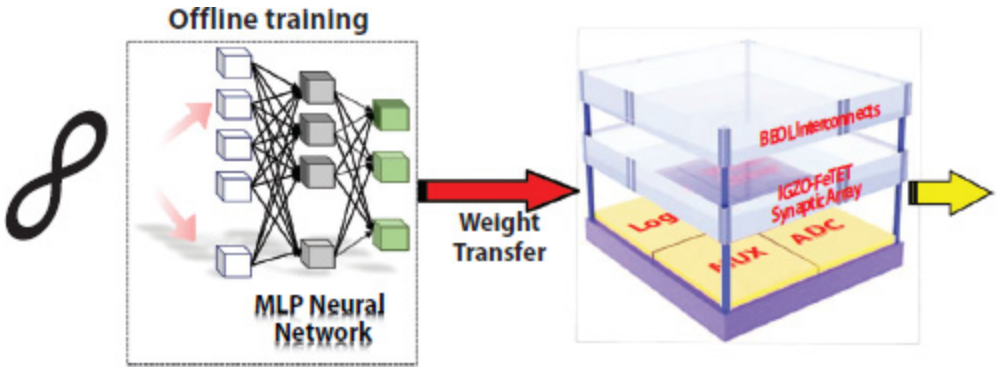

Figure 11.9 Architecture of proposed monolithic 3D-inference engine.

11.5 Conclusion

Recent progress in the research of hafnium oxide ($Hf\,O_2$) based FeFETs, FefinFETs, and FeTFTs has paved the way for further scaling and monolithic 3D-integration of Fe memory devices. In this work, we demonstrate IGZO based synaptic devices with an $8F_2$ feature size and lifelong retention, which is the most important characteristics for inference engines. IGZO based TFTs demonstrate multi-level coding operation, with retention for each state above ten years. We have further evaluated the performance of the IGZO-TFT as synaptic devices for monolithic 3D inference engines. The performance of these synaptic devices in terms of area and energy efficiency demonstrates the suitability of this device for IMC applications (Figure 11.10). The synaptic devices were capable of maintaining an inference accuracy above 95% for MNIST dataset recognition for ten years for multi-layer perceptron-based neural networks without re-training. Finally, Table 11.1 compares the performance of this device with other *state-of-art* synaptic devices.

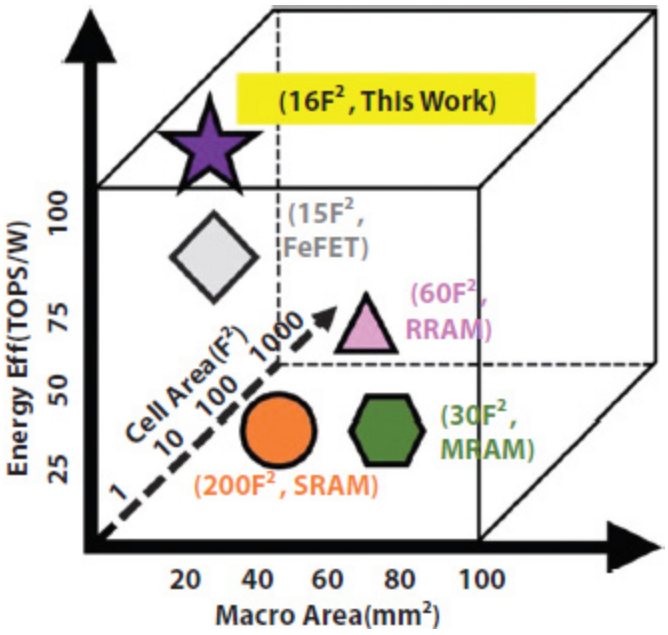

Figure 11.10 Comparison of FeTFT devices with other *State-of-Art* synaptic devices.

Table 11.1 Benchmarking table.

Device type	**Fe-FinFET [88]**	**IWO-FeFET [82]**	**IZTO-FeTFT [77]**	**IGZO-TFT [36]**
M3D Integrator	No	Yes	Yes	Yes
Cell Area (F^2)	$15F^2$	$15F^2$	$8F^2$	$8F^2$
R_{on} (Ω)	100K	4M	10K	100M
MW @10 Years	1	0.2	NA	1
Inference Accuracy Drop @ 10 Years	85%	85%	NA	1.5%
Energy Efficiency (TOPS/W)	N/A	71.04	NA	95.33

References

[1] R. Barfield, “Who invented computers?” 2020.

[2] I. J. Goodfellow and A. C. Yoshua Bengio, “Deep Learning [draft of March 30, 2015]-MIT Press (2016),” 2015.

[3] J. Sowa, V. Research, and S. Web, “Building Large Knowledge-Based Systems: Representation and Inference in the Cyc Project *,” no. December 2014.

[4] D. E. Rumelhart, G. E. Hinton, and R. J. Williams, “Learning representations by back-propagating errors,” *Nature*, vol. 323, no. 6088, 1986.

[5] Y. Lecun, Y. Bengio, and G. Hinton, “Deep learning,” *Nature*, vol. 521, no. 7553, pp. 436–444, 2015. [Online]. Available: https://doi.org/10.1038/nature14539

[6] Y. Lecun, L. Bottou, Y. Bengio, and P. Haffner, “Gradient-based learning applied to document recognition,” *Proceedings of the IEEE*, vol. 86, no. 11, pp. 2278–2324, 1998.

[7] K. Fukushima, “Neocognitron: A hierarchical neural network capable of visual pat- tern recognition,” *Neural Networks*, vol. 1, no. 2, pp. 119–130, 1988. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0893608088900147

[8] M. Riesenhuber and T. Poggio, “Hierarchical models of object recognition in cortex,” *Nature Neuroscience*, vol. 2, no. 11, pp. 1019–1025, 1999. [Online]. Available: https://doi.org/10.1038/14819

[9] N. Mauduit, M. Duranton, J. Gobert, and J.-A. Sirat, “Lneuro 1.0: a piece of hardware lego for building neural network systems,” *IEEE Transactions on Neural Networks*, vol. 3, no. 3, pp. 414–422, 1992.

[10] Eberhardt, Duong, and Thakoor, “Design of parallel hardware neural network systems from custom analog vlsi ’building block’ chips,” in *International 1989 Joint Conference on Neural Networks*, 1989, pp. 183–190 vol.2.

[11] P. Mazumder and Y.-S. Jih, “A new built-in self-repair approach to vlsi memory yield enhancement by using neural-type circuits,” *IEEE*

Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 12, no. 1, pp. 124–136, 1993.

[12] Y. Maeda, H. Hirano, and Y. Kanata, “A learning rule of neural networks via simultaneous perturbation and its hardware implementation,” *Neural Networks*, vol. 8, no. 2, pp. 251–259, 1995. [Online]. Available: https://www.sciencedirect.com/science/article/pii/089360809400084Y

[13] T. Gokmen and Y. Vlasov, “Acceleration of Deep Neural Network Training with Resistive Cross-Point Devices: Design Considerations,” *Frontiers in Neuroscience*, vol. 10, p. 333, 2016. [Online]. Available: https://www.frontiersin.org/article/10.3389/fnins.2016.00333

[14] S. Ambrogio, P. Narayanan, H. Tsai, R. M. Shelby, I. Boybat, C. di Nolfo, S. Sidler, M. Giordano, M. Bodini, N. C. P. Farinha, B. Killeen, C. Cheng, Y. Jaoudi, and G. W. Burr, “Equivalent-accuracy accelerated neural-network training using analogue memory,” *Nature*, vol. 558, no. 7708, pp. 60–67, 2018. [Online]. Available: https://doi.org/10.1038/s41586-018-0180-5

[15] J. Bae, S. Lim, B. Park, and J. Lee, “High-density and near-linear synaptic device based on a reconfigurable gated schottky diode,” *IEEE Electron Device Letters*, vol. 38, no. 8, pp. 1153–1156, 2017.

[16] C. Chang, P. Chen, T. Chou, I. Wang, B. Hudec, C. Chang, C. Tsai, T. Chang, and T. Hou, “Mitigating asymmetric nonlinear weight update effects in hardware neural network based on analog resistive synapse,” *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 8, no. 1, pp. 116–124, 2018.

[17] P. Chen, B. Lin, I. Wang, T. Hou, J. Ye, S. Vrudhula, J. Seo, Y. Cao, and S. Yu, “Mitigating effects of non- ideal synaptic device characteristics for on-chip learning,” in *2015 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2015, pp. 194–199.

[18] P. U. Diehl, D. Neil, J. Binas, M. Cook, S. Liu, and M. Pfeiffer, “Fast-classifying, high-accuracy spiking deep networks through weight and threshold balancing,” in *2015 International Joint Conference on Neural Networks (IJCNN)*, 2015, pp. 1–8.

[19] M. Ernoult, J. Grollier, and D. Querlioz, “Using Memristors for Robust Local Learning of Hardware Restricted Boltzmann Machines,” *Scientific Reports*, vol. 9, no. 1, p. 1851, 2019. [Online]. Available: https://doi.org/10.1038/s41598-018-38181-3

[20] J. Fu, Z. Liao, N. Gong, and J. Wang, “Mitigating nonlinear effect of memristive synaptic device for neuromorphic computing,” *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 9, no. 2, pp. 377–387, 2019.

[21] H. Kim, S. Hwang, J. Park, S. Yun, J. Lee, and B. Park, “Spiking neural network using synaptic transistors and neuron circuits for pattern recognition with noisy images,” *IEEE Electron Device Letters*, vol. 39, no. 4, pp. 630–633, 2018.

[22] J. Kim, J. Koo, T. Kim, and J.-J. Kim, “Efficient Synapse Memory Structure for Reconfigurable Digital Neuromorphic Hardware,” *Frontiers in Neuroscience*, vol. 12, p. 829, 2018. [Online]. Available: https://www.frontiersin.org/article/10.3389/fnins.2018.00829

[23] C. Kittel, “Theory of antiferroelectric crystals,” *Phys. Rev.*, vol. 82, pp. 729–732, Jun 1951. [Online]. Available: https://link.aps.org/doi/10.1103/PhysRev.82.729

[24] F. Akopyan, J. Sawada, A. Cassidy, R. Alvarez-Icaza, J. Arthur, P. Merolla, N. Imam, Y. Nakamura, P. Datta, G. Nam, B. Taba, M. Beakes, B. Brezzo, J. B. Kuang, R. Manohar, W. P. Risk, B. Jackson, and D. S. Modha, “Truenorth: Design and tool flow of a 65 mw 1 million neuron programmable neurosynaptic chip,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 34, no. 10, pp. 1537–1557, 2015.

[25] N. P. Jouppi, C. Young, N. Patil, D. Patterson, G. Agrawal, R. Bajwa, S. Bates, S. Bhatia, N. Boden, A. Borchers, R. Boyle, P. luc Cantin, C. Chao, C. Clark, J. Coriell, M. Daley, M. Dau, J. Dean, B. Gelb, T. V. Ghaemmaghami, R. Gottipati, W. Gulland, R. Hagmann, C. R. Ho, D. Hogberg, J. Hu, R. Hundt, D. Hurt, J. Ibarz, A. Jaffey, A. Jaworski, A. Kaplan, H. Khaitan, A. Koch, N. Kumar, S. Lacy, J. Laudon, J. Law, D. Le, C. Leary, Z. Liu, K. Lucke, A. Lundin, G. MacKean, A. Maggiore,

M. Mahony, K. Miller, Nagarajan, R. Narayanaswami, R. Ni, K. Nix, T. Norrie, M. Omernick, N. Penukonda, A. Phelps, and J. Ross, “In-datacenter performance analysis of a tensor processing unit,” 2017. [Online]. Available: https://arxiv.org/pdf/1704.04760.pdf

[26] C. Zhang, P. Li, G. Sun, Y. Guan, B. Xiao, and J. Cong, “Optimizing fpga-based accelerator design for deep convolutional neural networks,” in *Proceedings of the 2015 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, 2015, pp. 161–170.

[27] T. S. Böscke, “Ferroelektrische Speicherzelle, Herstellungsverfahren und integrierte Schaltung mit der fer- roelektrischen Speicherzelle,” Patent DE102 008 024 519B4.

[28] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, “Ferroelectricity in hafnium oxide thin films,” *Applied Physics Letters*, vol. 99, no. 10, p. 102903, 2011.

[29] X. Sang, E. D. Grimley, T. Schenk, U. Schr¨oder, and J. M. LeBeau, “On the structural origins of ferro- electricity in HfO2 thin films,” *Applied Physics Letters*, vol. 106, no. 16, p. 162905, 2015.

[30] S. De, F. Müller, H.-H. Le, M. Lederer, Y. Raffel, T. Ali, D. Lu, and T. Kämpfe, “Read-optimized 28nm hkmg multibit fefet synapses for inference-engine applications,” *IEEE Journal of the Electron Devices Society*, vol. 10, pp. 637–641, 2022.

[31] S. De, M. A. Baig, B.-H. Qiu, H.-H. Le, Y.-J. Lee, and D. Lu, “Neuromorphic computing with fe-finfets in the presence of variation,” in *2022 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)*, 2022, pp. 1–2.

[32] S. De, H.-H. Le, B.-H. Qiu, M. A. Baig, P.-J. Sung, C.-J. Su, Y.-J. Lee, and D. D. Lu, “Robust binary neural network operation from 233 k to 398 k via gate stack and bias optimization of ferroelectric finfet synapses,” *IEEE Electron Device Letters*, vol. 42, no. 8, pp. 1144–1147, 2021.

[33] S. De, F. Müller, N. Laleni, T. Soliman, A. Shrivastava, N. Yadav, S. Abdulazhanov, M. Lederer, Mojumder, A. Vardar, T. Ali, T. Kirchner, F.-

X. Liang, H.-H. Le, M. Baig, D. Lu, K. Seidel, and K¨ampfe, “First demonstration of ultra-high precision 4kb 28nm hkmg first demonstration of ultra-high precision 4kb 28nm hkmg 1fefet-1t based memory array macro for highly scaled 1fefet-1t based memory array macro for highly scaled deep learning applications deep learning applications.” [Online]. Available: https://doi.org/10.36227/techrxiv.19491212.v1

[34] S. De, B.-H. Qiu, W.-X. Bu, M. A. Baig, C.-J. Su, Y.-J. Lee, and D. Lu, “Neuromorphic computing with deeply scaled ferroelectric finfet in presence of process variation, device aging and flicker noise,” *ArxiV*, vol. abs/2103.13302, 2021. [Online]. Available: https://arxiv.org/abs/2103.13302

[35] S. De, M. A. Baig, B.-H. Qiu, F. Müller, H.-H. Le, M. Lederer, T. Kämpfe, T. Ali, P.-J. Sung, C.-J. Su, Y.-J. Lee, and D. D. Lu, “Random and systematic variation in nanoscale hf0.5zr0.5o2 ferroelectric finfets: Physical origin and neuromorphic circuit implications,” *Frontiers in Nanotechnology*, vol. 3, 2022. [Online]. Available: https://www.frontiersin.org/article/10.3389/fnano.2021.826232

[36] S. De, S. Thunder, D. Lehninger, H.-H. Le, Y. Raffel, M. Lederer, F. Müller, M. P. Jank, T.Ali, P.-T. Huang, K. Seidel, D. Lu, and T. Kämpfe, “Gate-stack engineered igzo-based multi-bit otp fetft with gate-stack engineered igzo-based multi-bit otp fetft with lifelong retention for inference engine applications lifelong retention for inference engine applications.” [Online]. Available: https://doi.org/10.36227/techrxiv.19491221.v2

[37] Y. Raffel, S. Thunder, M. Lederer, R. R. Olivo, R. Olivo, R. Hoffmann, L. Pirro, S. Beyer, T. Chohan, P.-T. Huang, S. De, T. Kämpfe, K. Seidel, and J. Heitmann, “Interfacial layer engineering to enhance endurance and noise immunity of fefets for imc applications high-k dielectrics doped with silicon and/or germanium for memory application view project interfacial layer engineering to enhance endurance and noise immunity of fefets for imc applications.” [Online]. Available: https://www.researchgate.net/publication/361048695

[38] T. D. Huan, V. Sharma, G. A. Rossetti, and R. Ramprasad, “Pathways towards ferroelectricity in hafnia,” *Physical Review B*, vol. 90, no. 6, p. 38, 2014.

[39] R. Materlik, C. Ku¨nneth, and A. Kersch, “The origin of ferroelectricity in Hf1 xZrxO2 : A computational investigation and a surface energy model,” *Journal of Applied Physics*, vol. 117, no. 13, p. 134109, 2015.

[40] M. Lederer, “Material development of doped hafnium oxide for nonvolatile ferroelectric memory application,” Ph.D. dissertation, Technische Universität Dresden, Dresden, 2022. [Online]. Available: https://nbn-resolving.org/urn:nbn:de:bsz:14-qucosa2-795729

[41] M. H. Park, Y. H. Lee, T. Mikolajick, U. Schröder, and C. S. Hwang, “Thermodynamic and Kinetic Origins of Ferroelectricity in Fluorite Structure Oxides,” *Advanced Electronic Materials*, vol. 99, p. 1800522, 2018.

[42] A. Toriumi, L. Xu, Y. Mori, X. Tian, P. D. Lomenzo, H. Mulaosmanovic, M. Materano, T. Mikolajick, and U. Schröder, “Material perspectives of HfO2-based ferroelectric films for device applications,” in *IEEE International Electron Devices Meeting*, ser. IEDM. IEEE, 2019, pp. 15.1.1–15.1.4.

[43] J. Müller, T. S. Böscke, U. Schröder, S. Müller, D. Bräuhaus, U. Böttger, L. Frey, and T. Mikolajick, “Ferroelectricity in Simple Binary ZrO2 and HfO2,” *Nano letters*, vol. 12, no. 8, pp. 4318–4323, 2012.

[44] J. Müller, U. Schröder, T. S. Böscke, I. Mu¨ller, U. Böttger, L. Wilde, J. Sundqvist, M. Lemberger, P. Kücher, T. Mikolajick, and L. Frey, “Ferroelectricity in yttrium-doped hafnium oxide,” *Journal of Applied Physics*, vol. 110, no. 11, p. 114113, 2011.

[45] S. Müller, J. Müller, A. Singh, S. Riedel, J. Sundqvist, U. Schröder, and T. Mikolajick, “Incipient Ferro- electricity in Al-Doped HfO2 Thin Films,” *Advanced Functional Materials*, vol. 22, no. 11, pp. 2412–2417, 2012.

[46] U. Schröder, E. Yurchuk, J. Müller, D. Martin, T. Schenk, P. Polakowski, C. Adelmann, M. I. Popovici, S. V. Kalinin, and T. Mikolajick, “Impact of different dopants on the switching properties of ferroelectric hafniumoxide,” *Japanese Journal of Applied Physics*, vol. 53, no. 8S1, p. 08LE02, 2014. [Online]. Available: http://stacks.iop.org/1347-4065/53/i=8S1/a=08LE02

[47] L. Xu, T. Nishimura, S. Shibayama, T. Yajima, S. Migita, and A. Toriumi, “Kinetic pathway of the ferroelectric phase formation in doped HfO2 films,” *Journal of Applied Physics*, vol. 122, no. 12, p. 124104, 2017.

[48] A. Toriumi, Y. Nakajima, and K. Kita, “(Invited) Opportunity for Phase-Controlled Higher-k HfO 2,” *ECS Transactions*, vol. 41, no. 7, pp. 125–136, 2011.

[49] M. H. Park, Y. H. Lee, H. J. Kim, T. Schenk, W. Lee, K. D. Kim, F. P. G. Fengler, T. Mikolajick, U. Schröder, and C. S. Hwang, “Surface and grain boundary energy as the key enabler of ferroelectricity in nanoscale hafniazirconia: A comparison of model and experiment,” *Nanoscale*, vol. 9, no. 28, pp. 9973–9986, 2017.

[50] M. Lederer, R. Olivo, D. Lehninger, S. Abdulazhanov, T. K¨ampfe, S. Kirbach, C. Mart, K. Seidel, and L. M. Eng, “On the Origin of Wake–Up and Antiferroelectric–Like Behavior in Ferroelectric Hafnium Oxide,” *physica status solidi (RRL)*, vol. 15, no. 5, p. 2100086, 2021.

[51] P. Polakowski and J. Müller, “Ferroelectricity in undoped hafnium oxide,” *Applied Physics Letters*, vol. 106, no. 23, p. 232905, 2015.

[52] M. Lederer, P. Bagul, D. Lehninger, K. Mertens, A. Reck, R. Olivo, T. Kämpfe, K. Seidel, and L. M. Eng, “Influence of Annealing Temperature on the Structural and Electrical Properties of Si-Doped Ferroelectric Hafnium Oxide,” *ACS Applied Electronic Materials*, 2021.

[53] H. Joh, T. Jung, and S. Jeon, “Stress Engineering as a Strategy to Achieve High Ferroelectricity in Thick Hafnia Using Interlayer,” *IEEE Transactions on Electron Devices*, vol. 68, no. 5, pp. 2538–2542, 2021.

[54] T. Shiraishi, K. Katayama, T. Yokouchi, T. Shimizu, T. Oikawa, O. Sakata, H. Uchida, Y. Imai, T. Kiguchi, T. J. Konno, and H. Funakubo, “Impact of mechanical stress on ferroelectricity in (Hf 0.5 Zr 0.5)O 2 thin films,” *Applied Physics Letters*, vol. 108, no. 26, p. 262904, 2016.

[55] A. Kruv, S. R. C. McMitchell, S. Clima, O. O. Okudur, N. Ronchi, G. van den Bosch, M. Gonzalez, I. de Wolf, and J. Houdt, “Impact of mechanical strain on wakeup of HfO2 ferroelectric memory,” in *IEEE International Reliability Physics Symposium (IRPS)*, ser. IRPS. IEEE, 2021, pp. 1–6.

[56] M. Lederer, K. Mertens, R. Olivo, K. Ku¨hnel, D. Lehninger, T. Ali, T. Kämpfe, K. Seidel, and L. M. Eng, “Substrate-dependent differences in ferroelectric behavior and phase diagram of Si-doped hafnium oxide,” *Journal of Materials Research*, 2021.

[57] F. Müller, M. Lederer, R. Olivo, T. Ali, R. Hoffmann, H. Mulaosmanovic, S. Beyer, S. Dünkel, J. Müller, S. Müller, K. Seidel, and G. Gerlach, “Current percolation path impacting switching behavior of ferroelectric FETs,” in *International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)*, ser. VLSI-TSA. IEEE, 2021, pp. 1–2.

[58] G. Choe and S. Yu, “Variability Analysis for Ferroelectric Field-Effect Transistors,” in *5th IEEE Electron Devices Technology & Manufacturing Conference (EDTM)*, ser. EDTM. IEEE, 2021, pp. 1–3.

[59] S. De, B.-H. Qiu, W.-X. Bu, M. A. Baig, P.-J. Sung, C.-J. Su, Y.-J. Lee, and D. D. Lu, “Uniform Crystal Formation and Electrical Variability Reduction in Hafnium-Oxide-Based Ferroelectric Memory by Thermal Engineering,” *ACS Applied Electronic Materials*, 2021.

[60] C. Garg, N. Chauhan, S. Deng, A. I. Khan, S. Dasgupta, A. Bulusu, and K. Ni, “Impact of Random Spatial Fluctuation in Non-Uniform Crystalline Phases on the Device Variation of Ferroelectric FET,” *IEEE Electron Device Letters*, vol. 42, no. 8, pp. 1160–1163, 2021.

[61] T. Ali, R. Olivo, S. Kerdilx00E8;s, D. Lehninger, M. Lederer, D. Sourav, A.-S. Royet, A. Sx00FC;nbx00FC;l, A. Prabhu, K. Kx00FC;hnel, M. Czernohorsky, M. Rudolph, R. Hoffmann, C. Charpin-

Nicolle, L. Grenouil- let, T. Kx00E4;mpfe, and K. Seidel, “Study of nanosecond laser annealing on silicon doped hafnium oxide film crystallization and capacitor reliability,” in *2022 IEEE International Memory Workshop (IMW)*, 2022, pp. 1–4.

[62] M. Lederer, T. K¨ampfe, R. Olivo, D. Lehninger, C. Mart, S. Kirbach, T. Ali, P. Polakowski, L. Roy, and K. Seidel, “Local crystallographic phase detection and texture mapping in ferroelectric Zr doped HfO2 films by transmission-EBSD,” *Applied Physics Letters*, vol. 115, no. 22, p. 222902, 2019.

[63] M. Lederer, D. Lehninger, S. Abdulazhanov, A. Reck, R. Olivo, T. Kampfe, and K. Seidel, “Process influences on the microstructure of BEoL integrated ferroelectric hafnium zirconium oxide,” in *2021 IEEE International Symposium on Applications of Ferroelectrics (ISAF)*. IEEE, 2021, pp. 1–4.

[64] M. Lederer, F. Müller, K. Kühnel, R. Olivo, K. Mertens, M. Trentzsch, S. Dünkel, J. Müller, S. Beyer, Seidel, T. Kämpfe, and L. M. Eng, “Integration of Hafnium Oxide on Epitaxial SiGe for p-type Ferro-electric FET Application,” *IEEE Electron Device Letters*, vol. 41, no. 12, pp. 1762–1765, 2020.

[65] M. Lederer, A. Reck, K. Mertens, R. Olivo, P. Bagul, A. Kia, B. Volkmann, T. Kämpfe, K. Seidel, and M. Eng, “Impact of the SiO 2 interface layer on the crystallographic texture of ferroelectric hafnium oxide,” *Applied Physics Letters*, vol. 118, no. 1, p. 012901, 2021.

[66] M. Lederer, T. Kämpfe, N. Vogel, D.Utess, B. Volkmann, T. Ali, R Olivo, J. Müller, S. Beyer, Trentzsch, K. Seidel, and L. M. Eng, “Structural and Electrical Comparison of Si and Zr Doped Hafnium Oxide Thin Films and Integrated FeFETs Utilizing Transmission Kikuchi Diffraction,” *Nanomaterials (Basel, Switzerland)*, vol. 10, no. 2, p. 384, 2020.

[67] F. Müller, M. Lederer, R. Olivo, A. Reck, T. Ali, K. Seidel, and T. Kampfe, “Microstructural implications for neuromorphic synapses based on ferroelectric hafnium oxide,” in *2021 IEEE International Symposium on Applications of Ferroelectrics (ISAF)*. IEEE, 2021, pp. 1–4.

[68] M. Lederer, F. Müller, A. Varanasi, R. Olivo, K. Mertens, D. Lehninger, Y. Raffel, R. Hoffmann, T. Ali, K. Seidel, T. K¨ampfe, and L. M. Eng, “Influence of microstructure on the variability and current percolation paths in ferroelectric hafnium oxide based neuromorphic FeFET synapses,” in *2021 Silicon Nanoelectronics Workshop (SNW)*, 2021, pp. 1–2.

[69] S. De, W.-X. Bu, B.-H. Qiu, C.-J. Su, Y.-J. Lee, and D. D. Lu, “Alleviation of charge trapping and flicker noise in hfzro2-based ferroelectric capacitors by thermal engineering,” in *2021 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)*, 2021, pp. 1–2.

[70] D. Lehninger, M. Ellinger, T. Ali, S. Li, K. Mertens, M. Lederer, R. Olivio, T. Kämpfe, N. Hanisch, K. Biedermann, M. Rudolph, V. Brackmann, S. Sanctis, M. P. M. Jank, and K. Seidel, “A fully integrated ferroelectric thin-film-transistor – influence of device scaling on threshold voltage compensation in displays,” *Advanced Electronic Materials*, vol. 7, no. 6, p. 2100082, 2021. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/aelm.202100082

[71] Y. Kato, Y. Kaneko, H. Tanaka, and Y. Shimada, “Nonvolatile Memory Using Epitaxially Grown Composite-Oxide-Film Technology,” *Japanese Journal of Applied Physics*, vol. 47, no. 4, pp. 2719–2724, 2008.

[72] M.-K. Kim and J.-S. Lee, “Ferroelectric Analog Synaptic Transistors,” *Nano letters*, vol. 19, no. 3, pp. 2044–2050, 2019.

[73] M.-K. Kim, I.-J. Kim, and J.-S. Lee, “CMOS-compatible ferroelectric NAND flash memory for high-density, low-power, and high-speed three-dimensional memory,” *Science Advances*, vol. 7, no. 3, p. eabe1341, 2021.

[74] F. Mo, Y. Tagawa, C. Jin, M. Ahn, T. Saraya, T. Hiramoto, and M. Kobayashi, “Experimental Demon- stration of Ferroelectric HfO 2 FET with Ultrathin-body IGZO for High-Density and Low-Power Memory Application,” in *IEEE Symposium on VLSI Technology*, ser. VLSI. IEEE, 2019, pp. T42–T43.

[75] J. Wu, F. Mo, T. Saraya, T. Hiramoto, M. Ochi, H. Goto, and M. Kobayashi, “Monolithic Integration of Oxide Semiconductor FET and Ferroelectric Capacitor Enabled by Sn-Doped InGaZnO for 3-D Embedded RAM Application,” *IEEE Transactions on Electron Devices*, vol. 68, no. 12, pp. 6617–6622, 2021.

[76] C. Sun, K. Han, S. Samanta, Q. Kong, J. Zhang, H. Xu, X. Wang, A. Kumar, C. Wang, Z. Zheng, X. Yin, K. Ni, and X. Gong, “Highly Scaled InGaZnO Ferroelectric Field-Effect Transistors and Ternary Content-Addressable Memory,” *IEEE Transactions on Electron Devices*, pp. 1–8, 2022.

[77] M.-K. Kim, I.-J. Kim, and J.-S. Lee, “Oxide semiconductor-based ferroelectric thin-film transistors for advanced neuromorphic computing,” *Applied Physics Letters*, vol. 118, no. 3, p. 032902, 2021.

[78] Y. Raffel, M. Lederer, R. Olivo, F. Mu¨ller, R. Hoffmann, T. Ali, T. Kämpfe, K. Seidel, and J. Heit- mann, “Charge pumping and flicker noise-based defect characterization in ferroelectric fets,” in *2020 IEEE International Integrated Reliability Workshop (IIRW)*, 2020, pp. 1–4.

[79] Y. Raffel, R. Olivo, M. Lederer, F. Mx00FC;ller, R. Hoffmann, T. Ali, K. Mertens, L. Pirro, M. Drescher, S. Beyer, T. K¨ampfe, K. Seidel, L. M. Eng, and J. Heitmann, “Endurance improvements and defect characterization in ferroelectric fets through interface fluorination,” in *2022 IEEE International Memory Workshop (IMW)*, 2022, pp. 1–4.

[80] Y. LeCun, Y. Bengio, and G. Hinton, “Deep learning,” *Nature*, vol. 521, no. 7553, pp. 436–444, 2015. [Online]. Available: https://doi.org/10.1038/nature14539

[81] S. De, M. Lederer, Y. Raffel, F. Müller, K. Seidel, and T. Kämpfe, “Roadmap for ferroelectric memory: Challenges and opportunities for imc applications,” *Internation SoC Conference, 2022*, 1 2022.

[82] S. Dutta, H. Ye, W. Chakraborty, Y.-C. Luo, M. S. Jose, B. Grisafe, A. Khanna, I. Lightcap, S. Shinde, S. Yu, and S. Datta, “Monolithic 3d integration of high endurance multi-bit ferroelectric fet for accelerating compute-in-memory,” in *2020 IEEE International Electron Devices Meeting (IEDM)*, 2020, pp. 36.4.1–36.4.4.

[83] D. D. Lu, S. De, M. A. Baig, B.-H. Qiu, and Y.-J. Lee, "Computationally efficient compact model for ferroelectric field-effect transistors to simulate the online training of neural networks," *Semiconductor Science and Technology*, vol. 35, p. 95007, 7 2020. [Online]. Available: https://doi.org/10.1088/1361-6641/ab9bed

[84] C.-W. Wang, H. Ku, C. Y. Chiu, S. De, B.-H. Qiu, C. Shin, and D. Lu, "Compact model for PZT ferroelectric capacitors with voltage dependent switching behavior," *Semiconductor Science and Technology*, vol. 35, p. 55033, 4 2020. [Online]. Available: https://doi.org/10.1088/1361-6641/ab7c79

[85] M. A. Baig, H.-H. Le, S. De, C.-W. Chang, C.-C. Hsieh, X.-S. Huang, Y.-J. Lee, and D. D. Lu, "Compact model of retention characteristics of ferroelectric FinFET synapse with MFIS gate stack," *Semiconductor Science and Technology*, vol. 37, p. 24001, 12 2021. [Online]. Available: https://doi.org/10.1088/1361-6641/ac3f22

[86] S. De, M. A. Baig, B.-H. Qiu, D. Lu, P.-J. Sung, F. Hsueh, Y.-J. Lee, and C.-J. Su, "Tri-gate ferroelectric fet characterization and modelling for online training of neural networks at room temperature and 233k," in *2020 Device Research Conference (DRC)*, 2020, pp. 1–2.

[87] S. De, Y.-J. Lee, and D. D. Lu, "Alleviation of temperature variation induced accuracy degradation in ferroelectric finfet based neural network," *arXiv e-prints*, pp. arXiv–2103, 2021.

[88] S. De, D. D. Lu, H.-H. Le, S. Mazumder, Y.-J. Lee, W.-C. Tseng, B.-H. Qiu, M. A. Baig, P.-J. Sung, C.- J. Su, C.-T. Wu, W.-F. Wu, W.-K. Yeh, and Y.-H. Wang, "Ultra-low power robust 3bit/cell $hf_{0.5}zr_{0.5}o_2$ ferroelectric finfet with high endurance for advanced computing-in-memory technology," in *2021 Symposium on VLSI Technology*, 2021, pp. 1–2.

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12
Radiation Effects and Their Impact on SRAM Design: A Comprehensive Survey with Contemporary Challenges

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Abstract

An extensive survey on several bit-cell Static Random Access Memory (SRAM) architectures and the effect of radiation induced faults and their related design concerns in deep sub-micron technologies is carried out in this chapter. It also compares SRAM topologies to radiation immune and variation tolerant SRAM structures. Variations of performance indices are presented and compared for different topologies as it is very difficult for a single topology to address all issues while operating at low voltages. The survey illustrates single event upsets (SEUs), single event multiple node upsets (SEMNUs), and cell stability metrics during the operation of various SRAM cells. All simulations are performed for various SRAM cells at 45nm with a power supply of 0.9V.

***Keywords*:** SRAM, low voltage, single event upsets, soft error rate, radiation hardened

12.1 Introduction

The Digital Revolution, analogous to the Industrial Revolution, brings the advent of the information age and a shift in technology to digital electronics from mechanical and analogue electronics [1]. The late 1950s to 1970s marks the beginning of this technological shift with the adoption and proliferation of digital computers. During and after the later half of the 20th

century, revolutionary changes were brought about in digital computing and digital information storage [2]. As technologies advanced, so did the need for more storage space with faster performance [3]. This led to transformations in digital storage devices from magnetic disks to optical and flash memory devices. Central to this revolution is the widespread usage and mass production of digital logic, MOSFETs, and silicon integrated circuit chips [4].

Advancements in silicon-based technology have changed day to day life. Developments in technology not only made human life more convenient with portable devices but also improved healthcare systems [5]. Recent improvements in artificial intelligence, Internet of Things (IoTs), communications, nanotechnology, and machine learning demand information processing to be on pace as described by Moore's Law, but exponential growth is now halted due to the demand for high computing capacities[6] [7]. The rise of big data is transforming networking and data storage capacities. Artificial Intelligence demands the best memory technology with fast access and low power consumption [8]. Memory bottlenecks limit the performance and energy in many System on Chips (SoC) [9], as a major portion of the SoC is occupied with on-chip static random access memory (SRAM) chips [10].

Portable microprocessor-based systems contain embedded memories [11]. Applications like intelligent wearable devices, space, military, wireless sensor networks, mobile and battery-operated devices, spatial electronics, and the Internet of Things need On-chip static random access memory (SRAMs) operating with low power and longer battery life [12] [13]. As stated by the International Technology Roadmap for Semiconductors (ITRS), SRAM occupies 90% of the chip area [14]. SRAMs also dominate the overall performance of the system. With improvements in technology, the speed of microprocessors is increasing by using the fastest memory that synchronizes with processor operation [15]. Due to its high compatibility with read/write logic, SRAM is becoming the paramount block in state-ofthe-art processors [16]. Technology scaling encouraged manufacturers to design smaller and faster memory that operates at low supply voltages [17]. In addition to this, designers must guarantee that the overall performance of the system is minimally affected [18].

Radiation effects are of major concern in SRAM circuits. Figure 12.1 illustrates single event upsets (SEUs) and single event multiple node upsets (SEMNUs) effects on the performance of SRAM during low voltage operation [19]. In this paper, a concise survey on several bit-cell SRAM architectures and radiation induced faults and mitigation techniques and their related design concerns in deep sub-micron technologies are discussed. The rest of the paper is organized as follows: Section 12.2 describes a literature survey on SRAM cells; radiation effects and their impact on performance metrics for SRAM topologies are discussed in Section 12.3; Section 12.4 discusses results and future scope; and Section 12.5 provides the conclusion of the paper.

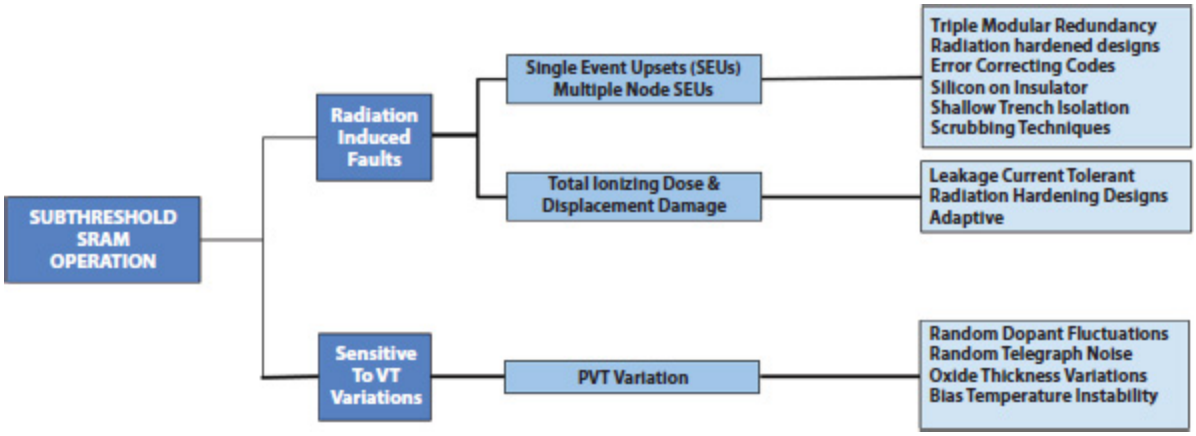

Figure 12.1 Subthreshold SRAM operational effects and improvement methods.

12.2 Literature Survey

Recent study states that SRAM cells are effected more by radiation induced soft errors due to low Q_{CRIT}, high integration density, and low supply voltage [20]. When a particle strikes the memory array it, may affect one or more transistors of the same or different memory cell, causing single event upsets (SEUs) and single event multiple node upsets (SEMNUs) [21]. SEMNUs occur due to angled particle striking that causes charge sharing and it creates multiple node upsets even in an SEU tolerant SRAM cell.

The Soft Error Rate (SER) can be reduced by using a transistor width modulation technique, but supply voltages must be kept near nominal, which is less preferred for low-voltage applications [22]. Soft error

mitigation techniques can be employed at the circuit level or architecture level [23]. SEU tolerant circuit hardening SRAM cell designs are classified based on their aerospace and terrestrial applications. [24] proposed two stacked SRAM architectures: NMOS stacked 10T SRAM and PMOS stacked 10T SRAM, but they provide only partial SEU immunity as they can recover only 0 to 1 and 1 to 0 upsets.

[25] proposed Quatro 10T which recovers 1 to 0 upsets only with negative feedback and the feedback affects the next node in the SRAM cell. [26] proposed radiation hardened by design (RHBD) 10T SRAM cells, which are best suited for aerospace applications. However, they have a penalty with read access times (RAT) and write access times (WAT). A dual interlocked storage cell (DICE) is also mostly used for latches and flip-flops and doesn't require an increase in the size of transistors and node capacitance. DICE is preferred even though it has area constraints because pass transistors are used for performing the write operation. Another design, Quatro, is more hardened than DICE, but it is observed that DICE offers lower SER than Quatro at lower linear energy transfers (LET) [27]. [28] proposed a differential read Quatro 10T which offers lower SER than Conv 6T and 1/2 rate error correcting code (ECC) protected 6T but suffers from high write failure probability. ECC is a conventional technique at the architecture level and it has greater time overheads due to encoding and decoding circuits, which is a drawback for terrestrial applications. [29] proposed a RHBD 10T SRAM cell and enhanced write access time compared to [28]. [3] combined word-line and bitline boosting techniques to enhance writability further under process variation when compared to [30]. A New Quatro-10T SRAM cell [31] is proposed that provides robustness from multinode upsets and improves write ability, read stability, and delay compared to the Quatro-10T proposed in [25].

[32] proposed a Quadruple Cross-Coupled Memory (QCCM)-10T SRAM cell that has better read stability, write ability, and immunity against SEUs and MNSEUs compared to the differential read Quatro 10T in [28]. Figure 12.2 compares the performance parameters of soft errors immune radiation hardened 10T SRAM cells among which RHBD10T [26] have least T_{WA} and T_{RA}, offering better performance and immunity to soft errors. [33] proposed an SEMNU tolerant 12T SRAM cell that Offers better performance when compared to [26], [34], [24], [25], [35], and [36] and

tolerates SEMNUs up to an LET of 62 Mevcm2 /mg. The We-Quatro 12T SRAM cell [37] is an extension of the Quatro cell that adds two extra access transistors to improve write ability, but it has low SER. A novel radiation hardened by polar design (RHPD) is fully tolerant to SEUs and improves performance compared to [37] and [36], which use 12T SRAM cells. A radiation hardened memory cell (RHMC)-12T reduced the number of sensitive nodes from 4 in [28] to 2, making it best suited for radiation environments [38].

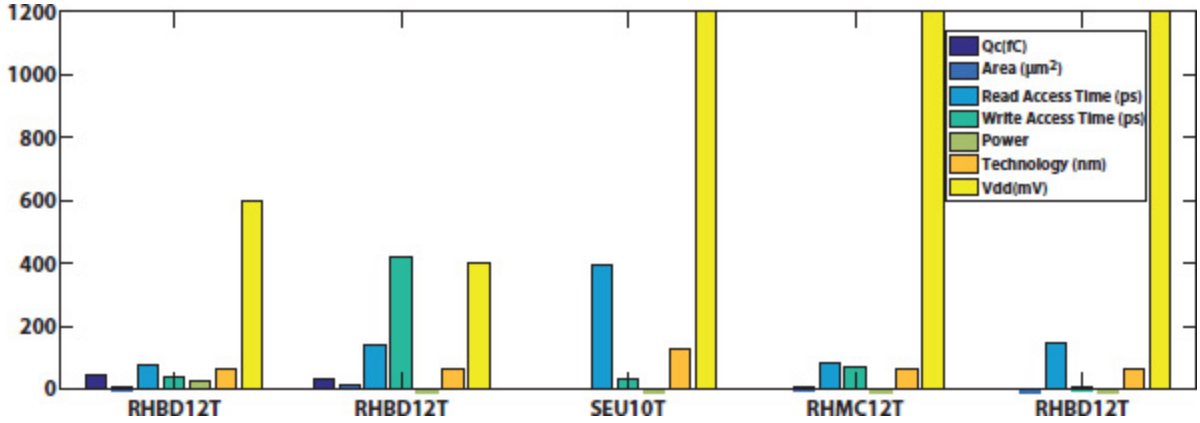

Figure 12.2 Comparative analysis of radiation hardened 12TSRAM cells: RHPD12T [20], RHBD12T [33], SETLU12T [39], RHMC12T [38], RHBD12T [35].

Total Ionizing Dose (TID) and displacement damage are gradual parametric degradations rather than abrupt functionality failures [40]. TID influence on multiple cell upsets is specified in [41]. TID in MOSFETs generates charge traps, decreasing the V_T of NMOS transistors, increasing leakage current, and degrading performance. TID response to various technologies is discussed in [42].

A novel energy efficient 12T SRAM improves radiation hardness, controlling cross coupled inverters using dummy pmos access devices, but write access time (WAT) is high when compared to [20]. It has better read access time (RAT), write access time (WAT), and critical charge. A soft error tolerant ultra-low Leakage 12T design [39] has better WAT and low leakage power because of stacking nmos transistors. To reduce SEUs, [38] proposed a technique identifying sensitive nodes, but it increases area overhead. A soft error immune SRAM cell designed using DG TFET

technology has the same stand-by power as a Conv6T but offers SEU immunity [43].

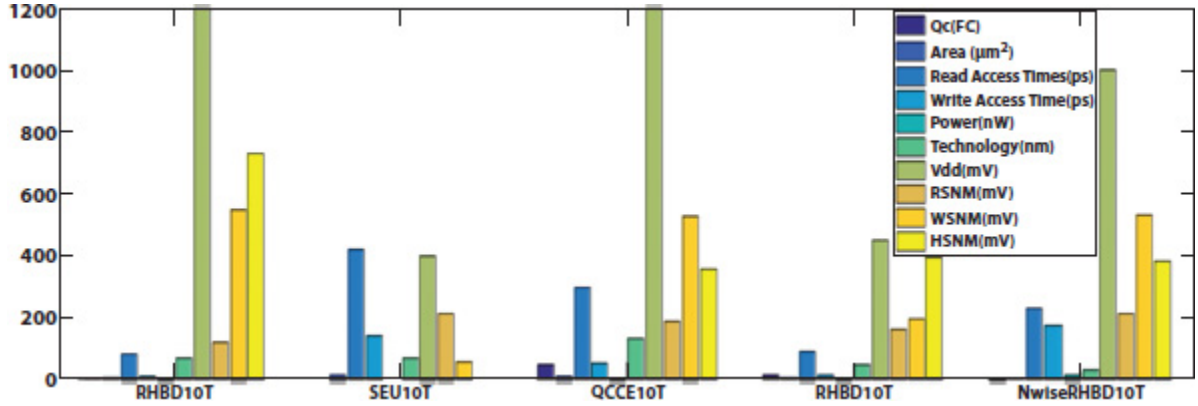

Figure 12.3 Comparative analysis of radiation hardened 10TSRAM cells: RHBD10T [26], SEU10T [33], QCCE10T [28], RHBD10T [3], Nwise10T [8].

Bit-Interleaving architecture also provides soft error immunity [44]. ECCs can detect/correct errors at the cost of area, power and delay. Figure 12.3 compares performance parameters of soft errors immune radiation hardened 12T SRAM cells among which RHPD12T [45] offers the least T_{WA} and T_{RA}, offering better performance and immunity to soft errors.

12.3 Impact of Radiation Effects on Sram Cells

Technology scaling encouraged manufacturers to design smaller and faster memory operating at low supply voltages. Supply voltage scaling for sub-threshold operation increases SRAMs' sensitivity to soft error rate (SER) [46]. Neutrons induced by cosmic radiation or alpha particles can change data in a memory cell even at sea-level applications [47]. Critical charge (Q_{CRIT}) is the minimum amount of charge deposited within the SRAM cell until induced current corrupts the stored data [48] [49]. The induced current $I_{ind}(t)$ [50] is defined as:

$$I_{ind}(t) = \frac{Q_{ind}}{t_f - t_r}\left(e^{\frac{t}{t_f}} - e^{\frac{t}{t_r}}\right) \tag{12.1}$$

where Q_{ind} is defined as the charge induced by the current pulse at the node and t_r and t_f are the rise and fall time constants. Induced charge Q_{ind} can be calculated by integrating the current at the node

after strike as:

$$Q_{ind} = \int_{t_r}^{t_f} I_{ind}(t)dt \tag{12.2}$$

Cell SER depends exponentially on the Q_{CRIT} [51]. SER decreases even for a slight increase in Q_{CRIT} [52]. SER is the only metric to evaluate the effect of radiation induced faults on integrated circuits. SER is denoted as:

$$SER = k\left(A_{diff,n} e^{Q_{crit,e}} + A_{diff,p} e^{Q_{crit,h}} \right) \tag{12.3}$$

$A_{diff,n}$ and $A_{diff,p}$ indicate the nmos and pmos sensitive drain areas, $Q_{crit,e}$ and $Q_{crit,h}$ are the critical charges due to electrons and holes, k depends on radiation flux, and η_e and η_h denote charge collection efficiency for holes and electrons. Q_{CRIT} due to collection of holes at the node required to flip data from ’0’ to ’1’ is

$$Q_{crit,h} \simeq (C_A V_{trip} + \zeta I_{DN} T_{pulse}) \tag{12.4}$$

C_A denotes equivalent capacitance at node A, V_{trip} is the threshold voltage at the node where the flip of data occurs, I_{DN} is defined as the maximum driving current of driving transistor M4, T_{pulse} is the time of particle induced current pulse, and ζ is the correction factor to calculate the time varying behavior of the restoring current. Similarly, the critical charge due to collection of holes at the node required to flip data from ’1’ to ’0’ is:

$$Q_{crit,e} \simeq (C_B V_{DD} - V_{trip} + |I_{DN}| T_{pulse}) \tag{12.5}$$

where C_B denotes equivalent capacitance at node B.

12.4 Results and Discussion

Simulations are performed using Cadence with a 45nm CMOS for analyzing various 10T and 12T SRAM topologies by considering radiation effects with supply voltage V_{DD}=0.9V at room temperature (27°C). Reverse-biased drain junction of transistors in the OFF state surrounds the sensitive nodes of the cell. When a radiation particle strikes a PMOS transistor, a positive transient is generated and, for the NMOS transistor, a negative transient pulse is induced. The single event upset due to particle strike is obtained by using a double exponential current source at sensitive nodes which are observed for flipping of data. It is modelled using Veriloga code in order to simulate its effect in Cadence Spectre. A six transistor SRAM cell [49] is most widely chosen for low power applications. It consists of two inverters forming a data latch which is used to store a single bit of information that can be accessed using two access transistors. The nodes that connect the data latch to the bit lines are Q and Qbar. By inducing a double exponential current source at one of the sensitive nodes (Qbar) and performing a transient simulation, as in shown in Figure 12.4, it is observed that the 6T SRAM cell is not tolerant to SEU and the voltage at the Qbar node is decreased, as shown in Figure 12.5.

Various radiation tolerant 10T SRAM cells are designed and simulated for immunity from particle strikes at single and multiple node upsets. It is observed in Figure 12.6 that the RHBD10T SRAM cell [29] uses an SEU recovery mechanism by temporarily gating transistors connected to the ground. The same can be observed when a transient simulation is performed.

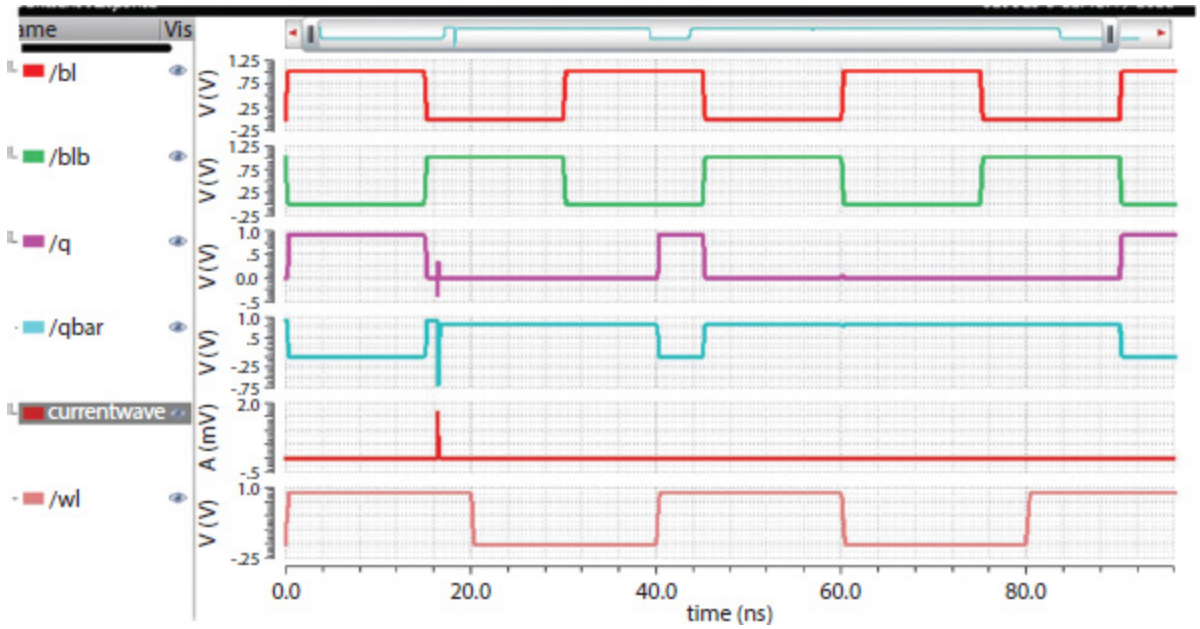

Figure 12.4 Transient simulation of 6T SRAM cell [49] with SEU induced at 16.5ns and operated at supply voltage (VDD=0.9V) [49].

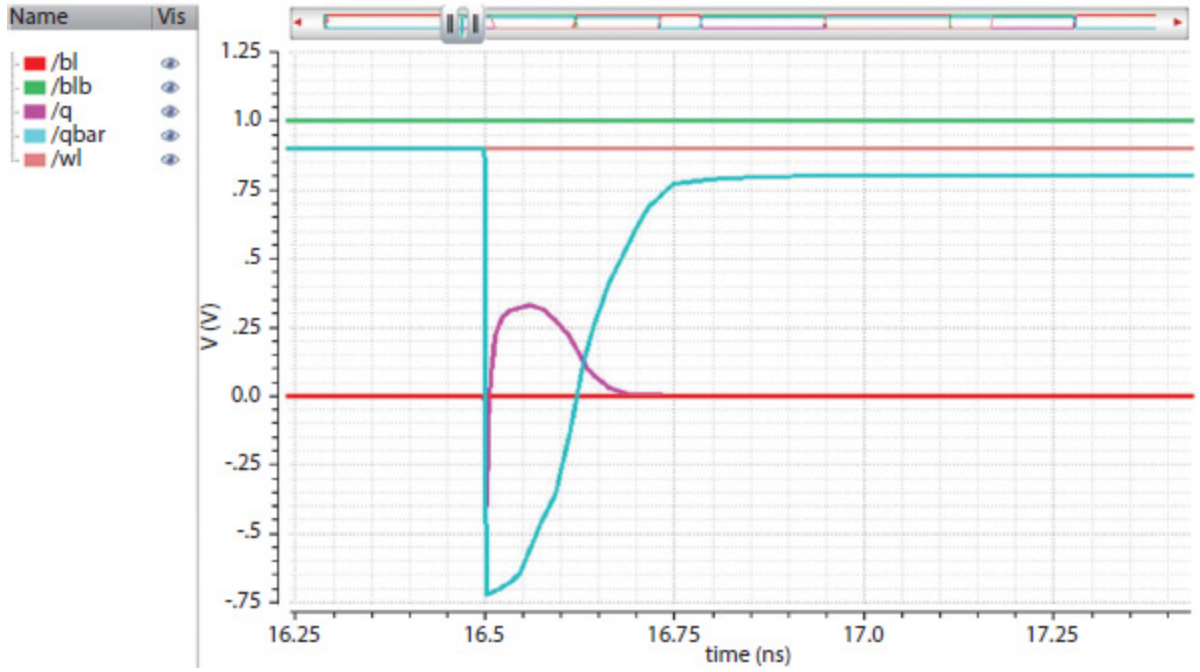

Figure 12.5 Effect of SEU on 6T SRAM CELL operating with supply voltage (VDD=0.9V).

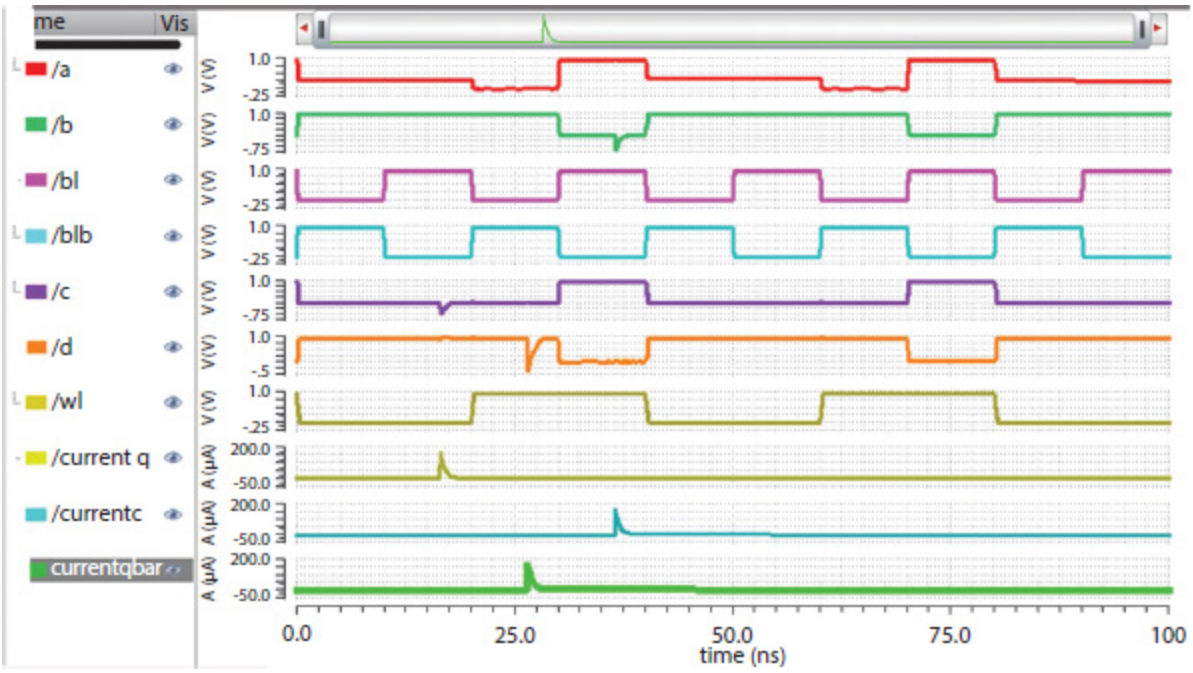

Figure 12.6 Effect of SEU on RHBD10T SRAM CELL [29] operating with supply voltage (VDD=0.9V) with supply voltage (V_{DD}=0.9V).

In the Nwise10T SRAM cell [8], the circuit has two feedback paths which help in easily recovering the initial state after particle strikes at storage nodes. Transient simulation of Nwise 10T SRAM cells is shown in Figure 12.7 and it is observed that when a double exponential current pulse is induced at 47ns, output storage node b recovers to its initial state making the design radiation hardened.

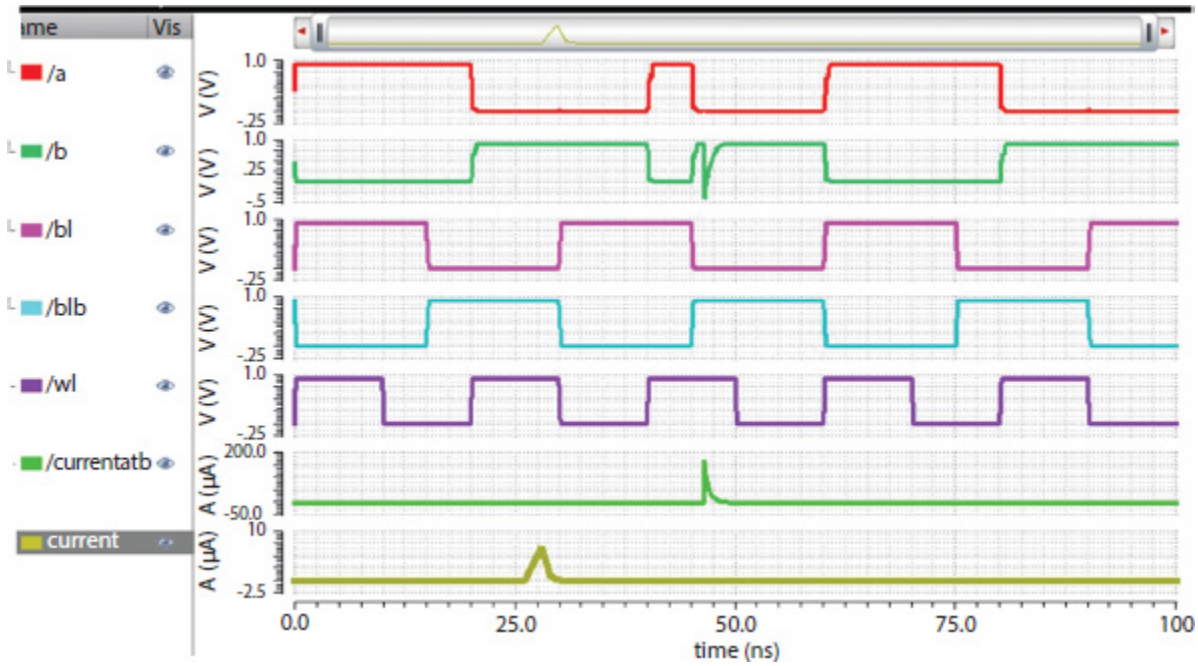

Figure 12.7 Effect of SEU on Nwise10T SRAM CELL [8] operating with supply voltage (VDD=0.9V).

Boosted WL and BL of a 10T SRAM cell [3] improves write ability and read stability under process variations. This is tested for soft error immunity, as shown in Figure 12.8, and it shows reliable operation over a wide range of frequencies. Quadruple cross-coupled storage cells (QUCCE) consist of two p-type and two n-type latch structures. All sensitive nodes of QUCCE 10T are affected by SEU and recover to their initial state. This structure provides better read and hold noise margins at a nominal supply voltage of 1.2V, as cited in [28], but the transient simulation performed in Figure 12.9 is performed at 45nm with V_{DD}=0.9V.

Among various 10T SRAM cells, the simulated Nwise 10T SRAM offers better soft error immunity when operated at low voltages and it also improves reliability by recovering back to the initial state. A novel energy efficient and higher SEMNU tolerant 12T SRAM cell [29] operating at near threshold region has lower susceptibility to SEU/SEMNU, a smaller read and write access time, and lesser area compared to other SRAM cells. The memory cell automatically corrects the errors as all four nodes are driven by a PMOS and an NMOS transistor and gate are connected to different nodes. Transient simulation of an SEU induced RHBD 12T SRAM cell is

shown in Figure 12.10. It can be observed that at 26.5ns, output storage node s1 recovers back to logic state ’1’.

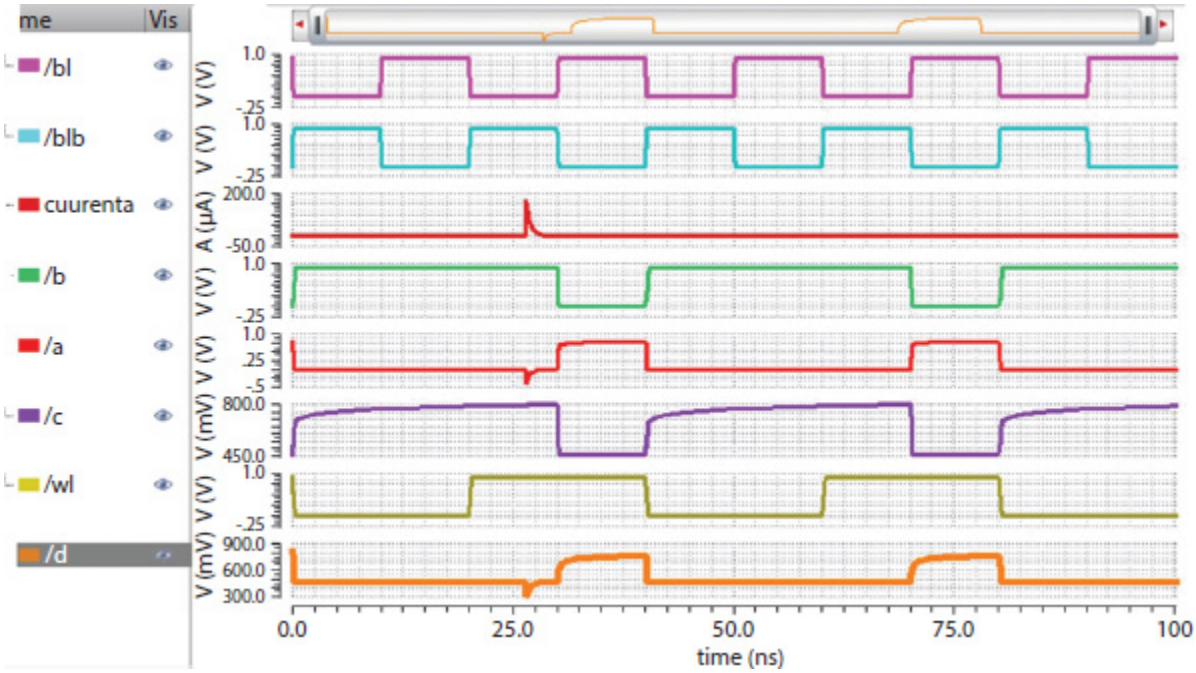

Figure 12.8 Effect of SEU on WL and BL boosted 10T SRAM CELL [3] operating with supply voltage (V_{DD}=0.9V).

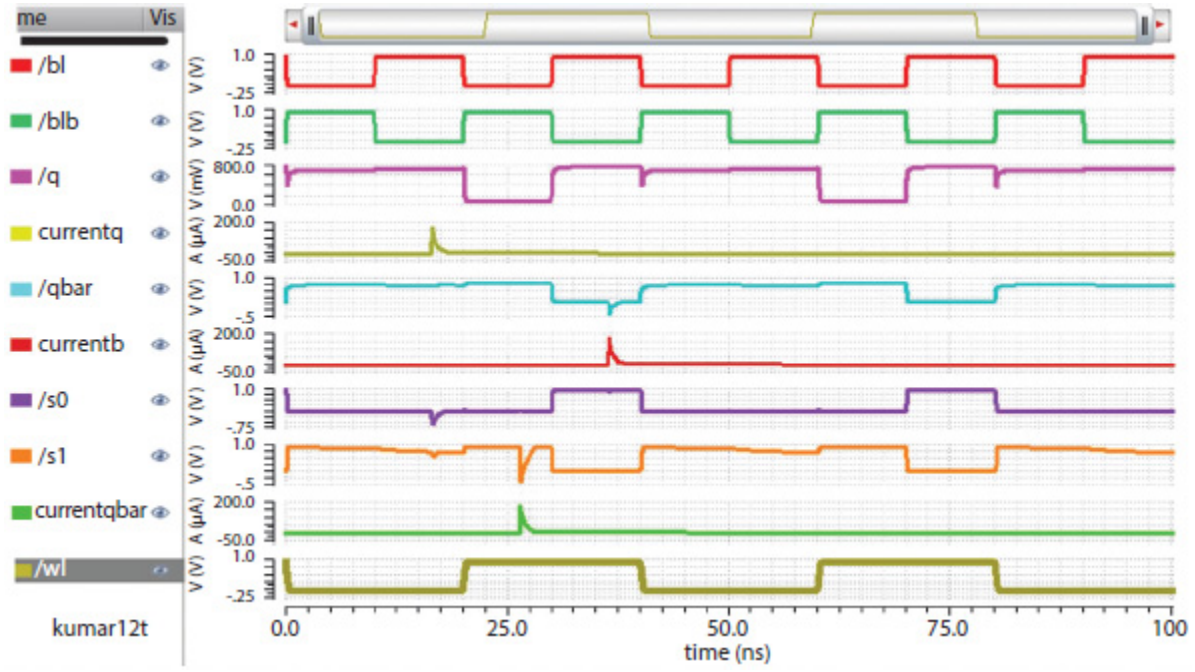

Figure 12.9 Effect of SEU on QCCE 10T SRAM CELL [28] operating with supply voltage (VDD=0.9V).

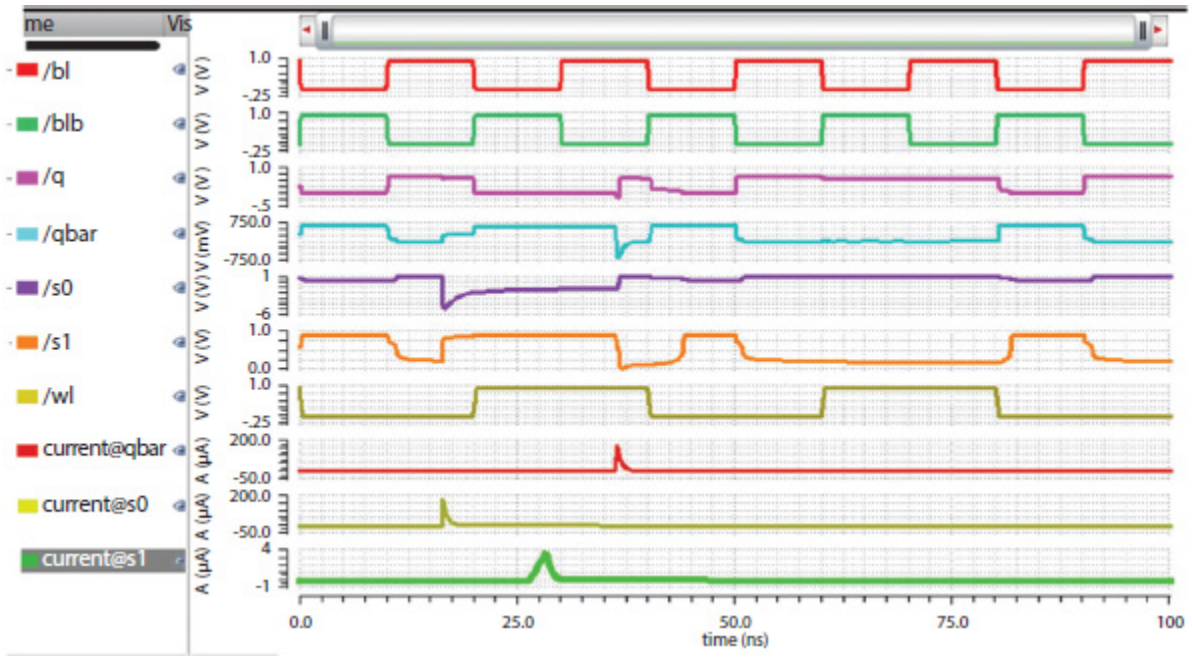

Figure 12.10 Effect of SEU on RHBD 12T SRAM CELL [29] operating with supply voltage (VDD=0.9V).

A QUCCE 12T SRAM cell consists of a cross-coupled latch structure which increases voltage difference between storage node pairs in the latch, increasing the voltage difference. It has a minimum critical charge and the least write access time is required, making it most suitable for soft error immune and high-performance memory applications. The result obtained in Figure 12.11 is simulated for SEU induced at all four nodes, providing high immunity at sub-threshold operation. It has four dominated leakage paths: two from bit-lines connected to the nodes storing '0' value to the ground through the active pull-down NMOS transistors and the other two from the power rail to ground through the disabled pull-down NMOS transistors.

A low leakage soft error tolerant SEU immune 12T SRAM cell [39] provides minimum critical charge with low leakage, as it uses stacked NMOS transistors which resist the leakage currents' nature to flow to the ground. But, it is observed that at low voltage applications, the data stored at internal nodes is affected, as in Figure 12.12 when simulated at 45nm technology with V_{DD}=0.9V.

A radiation hardened memory cell (RHMC) based 12T SRAM cell consists of four sensitive nodes and when a radiation particle strikes at one of the nodes, it changes its state from "1" to "0", turning on the PMOS transistor

and off the NMOS transistors, making the storage node Q float and vice versa for the Qbar nodes. This work was simulated at lower technology nodes, as shown in Figure 12.13, with an upset in data due to SEMNUs.

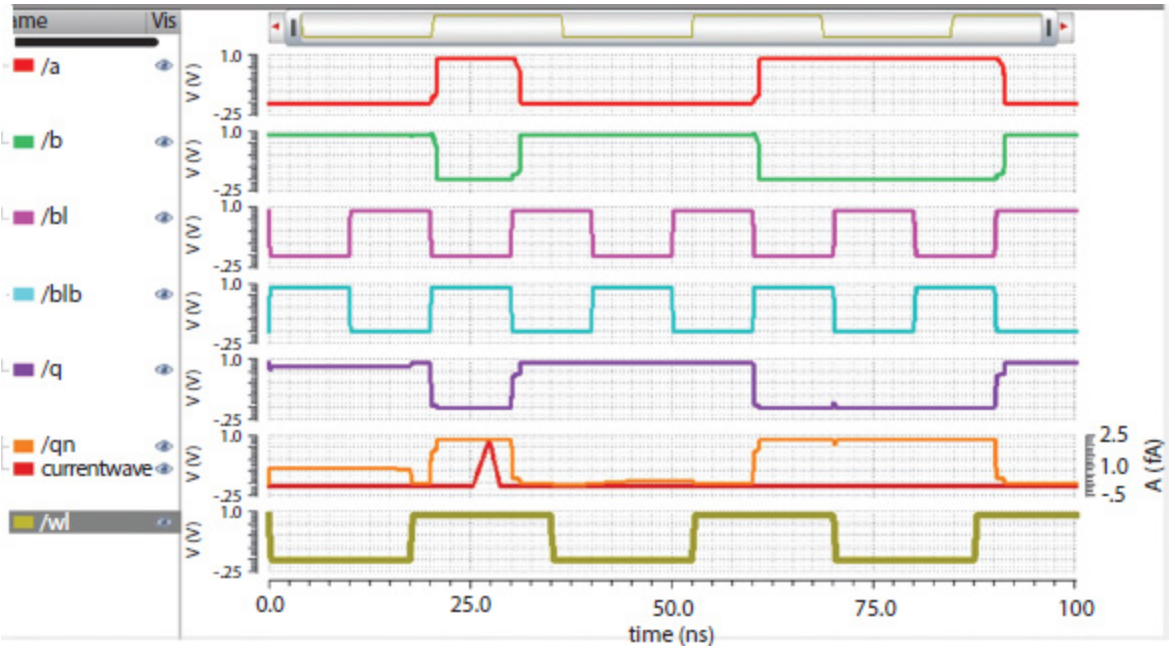

Figure 12.11 Effect of SEU on QCCE 12T SRAM CELL [28] operating with supply voltage (V_{DD}=0.9V).

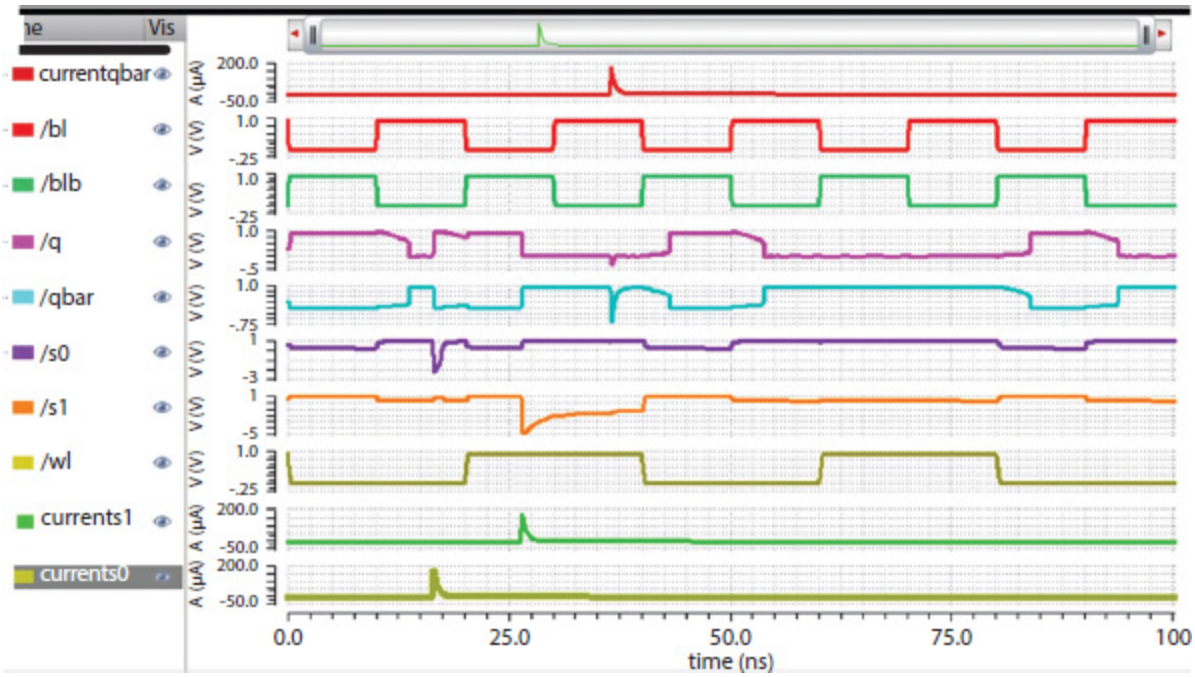

Figure 12.12 Transient simulation of low leakage SEU immune. 12T SRAM Cell [39] operated at supply voltage (V_{DD}=0.9V).

It is observed from various simulations, at a V_{DD} of 0.9V, that among various 12T SRAM cells simulated RHBD 12T SRAM cells [29] and Low leakage SEU immune 12T SRAM cells [39] are efficiently immune for both SEU and SEMNUs when operated for low voltage.

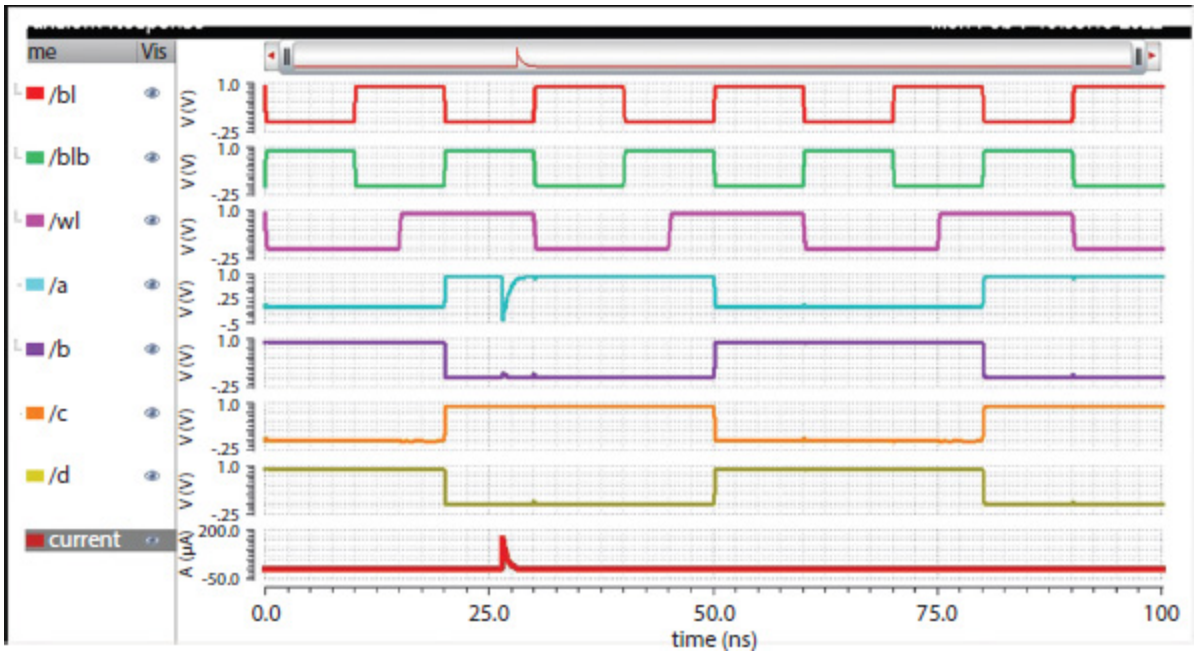

Figure 12.13 Transient simulation of 12T SRAM Cell [38] with SEU induced and operated at supply voltage V_{DD}=0.9V.

12.5 Conclusion

In this paper, All the simulations are carried out with 45nm technology with VDD=0.9V at 27°C. Various 10T and 12T SRAM cells are simulated for the effect of radiation faults by inducing a double exponential current source which causes storage nodes to flip from ’1’ to ’0’ and ’0’ to ’1’. Each of the radiation hardening architectures improves performance measures like cell stability and soft error immunity, making it a suitable SRAM design for low power and efficient applications. It is observed that each SRAM cell has its own advantages and is suited for various applications based on their requirements. For further research, various techniques used to improve RSNM and WSNM can be combined for low power and reliable SRAM cell design suitable for subthreshold operation.

Declarations

Data Availability

The authors confirm that the data supporting the findings of this study are available within the article, its supplementary materials, or below mentioned references.

References

1. J. B. Shaik, S. Singhal and N. Goel, Analysis of SRAM metrics for data dependent BTI degradation and process variability, *Integration* 72 (2020) 148–162.

2. T. S. Kumar and S. L. Tripathi, Leakage reduction in 18 nm FINFET based 7T SRAM cell using self controllable voltage level technique, *Wireless Personal Communications* (2020) 1–11.

3. G. Prasad, B. C. Mandi and M. Ali, Design and analysis of 10T-boosted radiation hardened SRAM cell for aerospace applications, in *2019 IEEE International Symposium on Smart Electronic Systems (iSES)(Formerly iNiS)*, IEEE2019, pp. 304–307.

4. H. Kumar and V. Tomar, Design of low power with expanded noise margin subthreshold 12T SRAM cell for ultra low power devices, *Journal of Circuits, Systems and Computers* (2020).

5. G. Torrens, B. Alorda, C. Carmona, D. Malagon-Perianez, J. Segura and S. A. Bota, A 65-nm reliable 6t cmos SRAM cell with minimum size transistors, *IEEE Transactions on Emerging Topics in Computing* (2017).

6. F. Al-Obaidy, A. Asad and F. A. Mohammadi, Improving powerperformance via hybrid cache for chip many cores based on neural network prediction technique, *Microsystem Technologies* (2020) 1–12.

7. C. Duari and S. Birla, Low leakage SRAM cell with improved stability for iot applications, *Procedia Computer Science* 171 (2020) 1469–1478.

8. A. Seyedi, S. Aunet and P. G. Kjeldsberg, Nwise: an area efficient and highly reliable radiation hardened memory cell designed for space applications, in *2019 IEEE Nordic Circuits and Systems Conference*

(NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC), IEEE2019, pp. 1–6.

9. S. Pal, S. Bose, W.-H. Ki and A. Islam, Half-select-free low-power dynamic loop-cutting write assist SRAM cell for space applications, *IEEE Transactions on Electron Devices* 67(1) (2019) 80–89.

10. T. Kim, K. Jeong, J. Choi, T. Kim and K. Choi, SRAM on-chip monitoring methodology for high yield and energy efficient memory operation at near threshold voltage, *Integration* (2020).

11. R. K. Maity, S. Tripathi, J. Samanta and J. Bhaumik, Lower complexity error location detection block of adjacent error correcting decoder for SRAMs, *IET Computers & Digital Techniques* (2020).

12. S. Pal, S. Bose and A. Islam, Design of sram cell for low power portable healthcare applications, *Microsystem Technologies* (2020) 1–12.

13. N. Surana and J. Mekie, Energy efficient single-ended 6-t SRAM for multimedia applications, *IEEE Transactions on Circuits and Systems II: Express Briefs* 66(6) (2018) 1023–1027.

14. S. Pal and A. Islam, Variation tolerant differential 8T SRAM cell for ultralow power applications, *IEEE transactions on computer-aided design of integrated circuits and systems* 35(4) (2015) 549–558.

15. D. Nayak, D. P. Acharya and K. Mahapatra, An improved energy efficient SRAM cell for access over a wide frequency range, *Solid-State Electronics* 126 (2016) 14–22.

16. R. Gupta and S. Dasgupta, Process corners analysis of data retention voltage (drv) for 6t, 8T, and 10T SRAM cells at 45 nm, *IETE Journal of Research* 65(1) (2019) 114–119.

17. C. Roy and A. Islam, Design of differential tg based 8t sram cell for ultralowpower applications, *Microsystem Technologies* (2018) 1–12.

18. G. Prasad and A. Anand, Statistical analysis of low-power SRAM cell structure, *Analog Integrated Circuits and Signal Processing* 82(1) (2015) 349–358.

19. S. Pal, S. Bose and A. Islam, A low power sram cell design for wireless sensor network applications, *Microsystem Technologies* (2019) 1–11.

20. Q. Zhao, C. Peng, J. Chen, Z. Lin and X. Wu, Novel write-enhanced and highly reliable rhpd-12T SRAM cells for space applications, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 28(3) (2020) 848–852.

21. D. Malagon, G. Torrens, J. Segura and S. A. Bota, Single event upsets´ characterization of 65 nm cmos 6t and 8T SRAM cells for ground level environment, *Microelectronics Reliability* 110 (2020) p. 113696.

22. G. Torrens, A. Alheyasat, B. Alorda, S. Barcelo, J. Segura and S. Bota,´ Transistor width effect on the power supply voltage dependence of α-ser in cmos 6t SRAM, *IEEE Transactions on Nuclear Science* 67(5) (2020) 811–817.

23. K. W. Gear, A. Sanchez-Maci´ an, F. Garcia-Herrero and J. A. Maestro,´ Two behavioural error detection techniques for the cascaded integrator–comb interpolation filter implemented on fpga, *Circuits, Systems, and Signal Processing* (2020) 1–14.

24. I.-S. Jung, Y.-B. Kim and F. Lombardi, A novel sort error hardened 10t sram cells for low voltage operation, in *2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, IEEE2012, pp. 714–717.

25. S. M. Jahinuzzaman, D. J. Rennie and M. Sachdev, A soft error tolerant 10t sram bit-cell with differential read capability, *IEEE Transactions on Nuclear Science* 56(6) (2009) 3768–3773.

26. J. Guo, L. Zhu, Y. Sun, H. Cao, H. Huang, T. Wang, C. Qi, R. Zhang, X. Cao, L. Xiao *et al.*, Design of area-efficient and highly reliable rhbd 10T memory cell for aerospace applications, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 26(5) (2018) 991–994.

27. Q. Wu, Y. Li, L. Chen, A. He, G. Guo, S. H. Baeg, H. Wang, R. Liu, L. Li, S.-J. Wen *et al.*, Supply voltage dependence of heavy ion induced sees on 65 nm cmos bulk SRAMs, *IEEE Transactions on Nuclear Science* 62(4) (2015) 1898–1904.

28. J. Jiang, Y. Xu, W. Zhu, J. Xiao and S. Zou, Quadruple cross-coupled latchbased 10T and 12T SRAM bit-cell designs for highly reliable terrestrial applications, *IEEE Transactions on Circuits and Systems I: Regular Papers* 66(3) (2018) 967–977.

29. C. Kumar and B. Anand, Design of highly reliable energy-efficient seu tolerant 10t sram cell, *Electronics Letters* 54(25) (2018) 1423–1424.

30. M. Kang, J. Kim, I.-J. Chang *et al.*, Studying the variation effects of radiation hardened quatro sram bit-cell, *IEEE Transactions on Nuclear Science* 63(4) (2016) 2399–2401.

31. L. Wen, Y. Zhang and P. Wang, Radiation-hardened, read-disturbancefree new-quatro-10t memory cell for aerospace applications, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 28(8) (2020) 1935–1939.

32. A. Yan, J. Zhou, Y. Hu, J. Cui, Z. Huang, P. Girard and X. Wen, Novel quadruple cross-coupled memory cell designs with protection against single event upsets and double-node upsets, *IEEE Access* 7 (2019) 176188–176196.

33. C. I. Kumar and B. Anand, A highly reliable and energy efficient radiation hardened 12T SRAM cell design, *IEEE Transactions on Device and Materials Reliability* 20(1) (2019) 58–66.

34. C. Qi, L. Xiao, T. Wang, J. Li and L. Li, A highly reliable memory cell design combined with layout-level approach to tolerant single-event upsets, *IEEE Transactions on Device and Materials Reliability* 16(3) (2016) 388–395.

35. J. Guo, L. Zhu, W. Liu, H. Huang, S. Liu, T. Wang, L. Xiao and Z. Mao, Novel radiation-hardened-by-design (rhbd) 12T memory cell for aerospace applications in nanoscale cmos technology, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 25(5) (2017) 1593– 1600.

36. T. Calin, M. Nicolaidis and R. Velazco, Upset hardened memory design for submicron cmos technology, *IEEE Transactions on nuclear science* 43(6) (1996) 2874–2878.

37. J. S. Kim, I. J. Chang *et al.*, We-quatro: Radiation-hardened sram cell with parametric process variation tolerance, *IEEE Transactions on Nuclear Science* 64(9) (2017) 2489–2496.

38. S. Dohar, R. Siddharth, M. Vasantha and N. K. YB, A novel single event upset tolerant 12T memory cell for aerospace applications, in *2020 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, IEEE2020, pp. 48–53.

39. J. Jiang, D. Lin, J. Xiao and S. Zou, Soft-error-tolerant ultralow-leakage 12T SRAM bitcell design, in *2019 International Conference on IC Design and Technology (ICICDT)*, IEEE2019, pp. 1–2.

40. C. Calligaro and U. Gatti, Rad-hard mixed-signal ic design, theory and implementation, in *Next-Generation ADCs, High-Performance Power Management, and Technology Considerations for Advanced Integrated Circuits*, (Springer, 2020) pp. 273–297.

41. Q. Zheng, J. Cui, W. Lu, H. Guo, J. Liu, X. Yu, L. Wang, J. Liu, C. He, D. Ren *et al.*, Total ionizing dose influence on the single-event multiplecell upsets in 65-nm 6-t sram, *IEEE Transactions on Nuclear Science* 66(6) (2018) 892–898.

42. E. Chatzikyriakou, K. Morgan and C. K. De Groot, Total ionizing dose hardened and mitigation strategies in deep submicrometer cmos and beyond, *IEEE Transactions on Electron Devices* 65(3) (2018) 808–819.

43. M. Pown and B. Lakshmi, Investigation of radiation hardened tfet SRAM cell for mitigation of single event upset, *IEEE Journal of the Electron Devices Society* (2020).

44. D. Nayak, D. P. Acharya, P. K. Rout and U. Nanda, A high stable 8TSRAM with bit interleaving capability for minimization of soft error rate, *Microelectronics Journal* 73 (2018) 43–51.

45. G. Prasad, B. C. Mandi and M. Ali, Power optimized SRAM cell with high radiation hardened for aerospace applications, *Microelectronics Journal* (2020) p. 104843.

46. M. S. Aghadadi, M. Fazeli and H. Beitollahi, Joint effects of aging and process variations on soft error rate of nano-scale digital circuits, *Journal of Circuits, Systems and Computers* (2020) p. 2150012.

47. G. Torrens, S. A. Bota, B. Alorda and J. Segura, An experimental approach to accurate alpha-ser modeling and optimization through design parameters in 6t SRAM cells for deep-nanometer cmos, *IEEE Transactions on Device and Materials Reliability* 14(4) (2014) 1013–1021.

48. V. M. Van Santen, J. Martin-Martinez, H. Amrouch, M. M. Nafria and J. Henkel, Reliability in super-and near-threshold computing: A unified model of rtn, bti, and pv, *IEEE Transactions on Circuits and Systems I: Regular Papers* 65(1) (2017) 293–306.

49. R. Saeidi, M. Sharifkhani and K. Hajsadeghi, A subthreshold symmetric SRAM cell with high read stability, *IEEE Transactions on Circuits and Systems II: Express Briefs* 61(1) (2014) 26–30.

50. H. Mostafa, M. Anis and M. Elmasry, A design-oriented soft error rate variation model accounting for both die-to-die and within-die variations in sub-micrometer cmos SRAM cells, *IEEE Transactions on Circuits and Systems I: Regular Papers* 57(6) (2010) 1298–1311.

51. N. Gupta, A. P. Shah, R. S. Kumar, T. Gupta, S. Khan and S. K. Vishvakarma, On-chip adaptive vdd scaled architecture of reliable SRAM cell with improved soft error tolerance, *IEEE Transactions on Device and Materials Reliability* (2020).

52. T. Heijmen, P. Roche, G. Gasiot, K. R. Forbes and D. Giot, A comprehensive study on the soft-error rate of flip-flops from 90-nm production libraries, *IEEE Transactions on Device and Materials Reliability* 7(1) (2007) 84–96.

Note

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13
Final Summary and Future of Advanced Ultra Low Power Metal Oxide Semiconductor Field Effect Transistors

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Abstract

So far, various state-of-art techniques have been widely addressed to design ultra-low power semiconductors. Doping technique (TFET, junctionless transistor), oxide material technique (NCFET, ferroelectric), gate metal material technique (gate engineered-TFET, heterogate structure), and structural engineering (FinFET, NSFET, GAA MOSFET) have been discussed to lower subthreshold swing (SS), thereby realizing ultra-low power semiconductor design. However, all these cutting-edge technologies have one common characteristic, namely an increase in production cost. As more complex structures are introduced to achieve ultra-low power consumption, more complex production processes are concomitantly required, meaning cost increases and fabrication failures could inevitably

arise. In this regard, this final chapter will explain the challenges of futuristic device structures and the future of ultra-low power metal oxide semiconductor field effect transistors (MOSFET).

***Keywords*:** Semiconductor, Fabrication, Cost, Yield Rate, Low Power Consumption, Futuristic Semiconductor, Next-Generation Semiconductor

13.1 Introduction

In a general sense, it has been a rule of thumb to change the structure and material of transistors, thereby realizing high performance and low power consumption [1-4]. To validate these demands for material and structural change, countless research has been broadly conducted by mathematical analysis, modelling, and fabrication [5-7]. From a structural point of view, as shown in Figure 13.1, the structure of the metal oxide semiconductor field effect transistor (MOSFET) has evolved from a planar structure to a double gate structure, to a FinFET structure, to a gate-all-around (GAA) MOSFET structure (also known as a Nanosheet (NS) FET structure) [8]. Whenever this structural evolution was realized, more complex fabrication processes and advanced fabrication-equipment were needed, which inevitably increases the fabrication cost [9]. In addition, the yield rate (the ratio of successful microchips among all of the produced microchips) somewhat steadily decreased, which has induced so much demand for reliability research [10].

At the same time, it is also important to look over the practicality of cutting-edge technology. Let's take heterogate structure (described in the previous chapter) for example [Figure 13.2] [11-16]. This heterogate structure might only be possible to fabricate, only if half of the gate length (L_{gate}) could be actually realized by existing production facilities (technically, EUV facilities or e-beam facility). Of course, this heterogate structure is a viable structure in 3/5/7-nm technology, which has enabled transistors to be steadily developed [17, 18]. However, later on, if technology nodes develop and L_{gate} becomes lower than 8 nm, this structure might be faced with various fabrication issues and yield-rate issues [19].

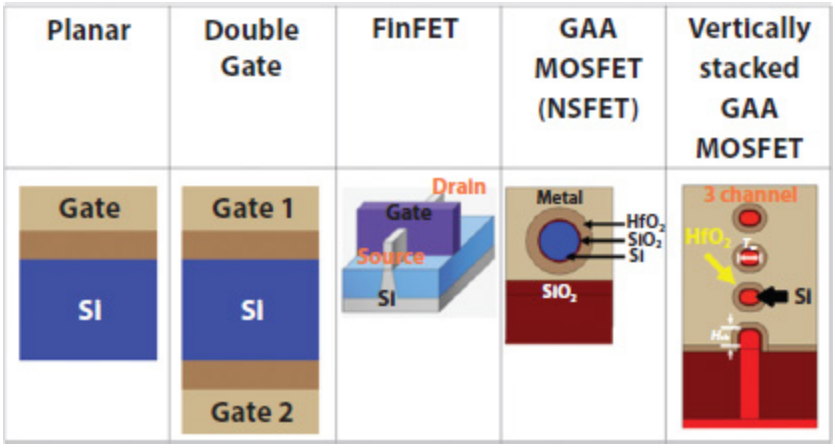

Figure 13.1 Structure evolution of transistor (from planar MOSFET, via FinFET, to stacked GAA MOSFET).

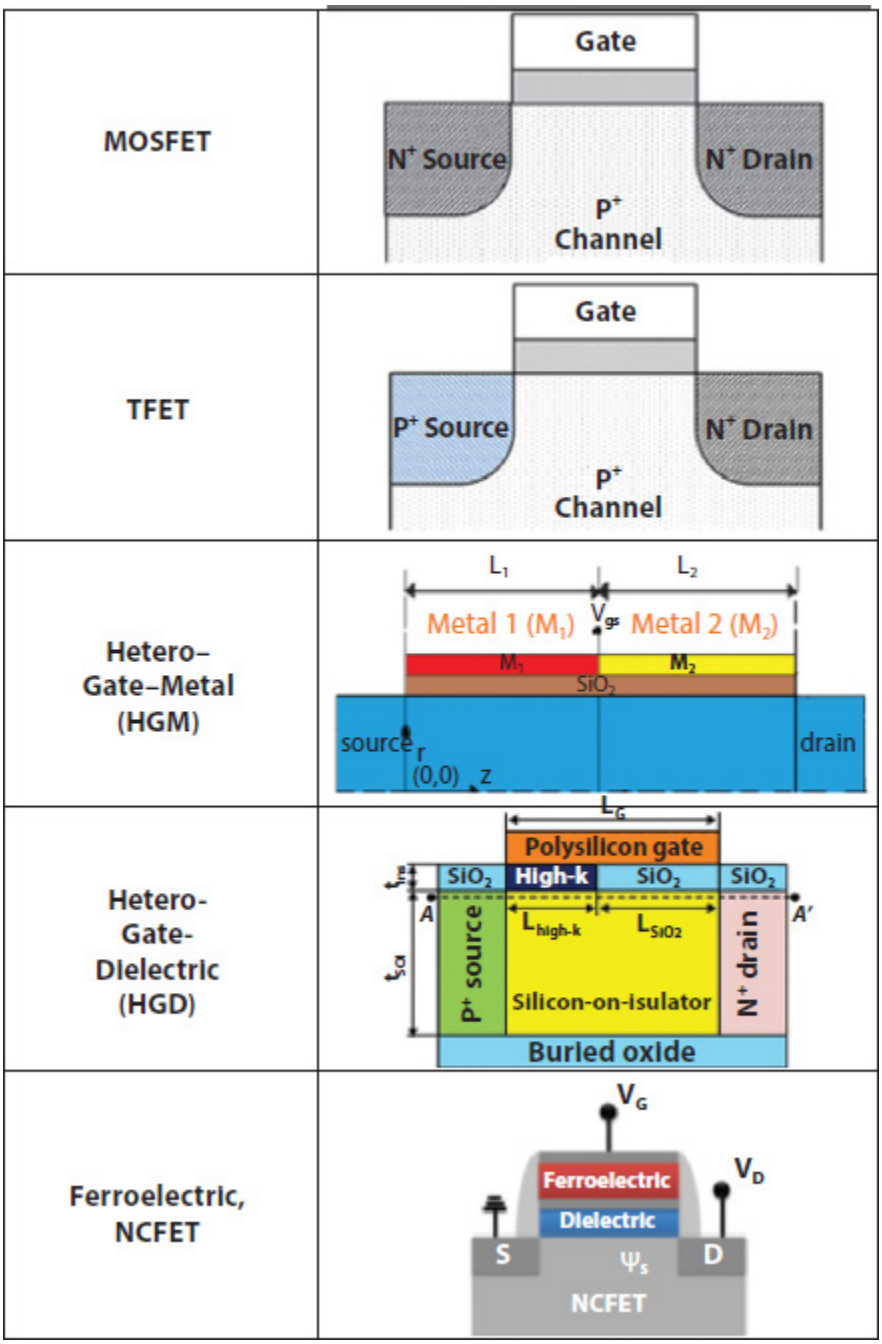

Figure 13.2 Material evolution of transistor.

Therefore, practicality, productivity, punctuality, and profitability (4P) would be the engineer's first concerns and the most important considerations in semiconductor engineering. In this regard, future challenges and issues of various structures will be covered in this final chapter.

13.2 Challenges in Future Ultra-Low Power Semiconductors

Tables 13.1 and 13.2 explain the overall evaluation of structural engineering and material engineering [20, 21]. As described in Table 13.1, each structural evolution has advantages and disadvantages. For example, when the device structure evolves from planar MOSFET to double gate MOSFET, there is a slight cost increase due to an increase in the fabrication process [22]. The authors believe that the reader could easily understand this because double gate structure means that there are 'two' gates. Then, compared to planar MOSFET, one additional gate and gate dielectric layer must be additionally formed in double gate MOSFET, which might cause a cost increase [23].

Next, when the device structure evolved from double gate MOSFET to FinFET, several yield-rate issues arose [24]. For example, the shape of the channel in FinFET is obviously a fin shape (such as shark fin, dolphin fin) [24]. This fin-shaped channel makes FinFET hard to fabricate [24]. Specifically, when manufacturers try to fabricate this FinFET with mass production, there could be a 'triangle-shaped channel' rather than a 'finshaped channel' [25]. Then, the area of the channel might decrease which brings a low on-current (I_{ON}) and performance failure (technically, this effect has been called 'edge-effect' or 'corner-effect') [26, 27].

Table 13.1 Overview of disadvantages and advantages of structure engineering.

Structural engineering	Disadvantage		Advantage		Location
	Cost increase	Yield-rate increase	Purpose	Result	Chapter in this book
Planar MOSFET	-	-	-	High I_{ON} & low I_{OFF}	1, 2, 13
Double Gate MOSFET	Δ (low)	-	Low Power Consumption		13
FinFET	Δ (low)	Δ (low)	High Integration		13
GAA MOSFET	O (high)	OO (very high)	Low Power Consumption		9
Vertically Stacked GAA MOSFET	OO (very high)	OO (very high)	High Performance		9

The most important consideration comes next. Especially when transistor structure evolved from FinFET to GAA MOSFET, yield-rate issues seriously arose [28, 29]. For details, let's take a look at Figure 13.3 (Figure 13.3 is and edited figure, the original figure can be found in the previous research done by J. J. Gu from Purdue University [30]).

As shown in Figure 13.3, the fabrication process became much more complicated when the transistor structure evolved from FinFET to GAA MOSFET and vertically stacked GAA MOSFET [31-34]. Especially since GAA MOSFET requires airborne channel structure during fabrication (see three airborne channels in 'Step 6' of Figure 13.3), Si/Ge/Si/Ge/Si layers should be initially formed (see 'Step 2' of Figure 13.3) [30]. These Si/Ge/Si/ Ge/Si layers are normally formed by the epitaxy process [30]. In particular, this epitaxy process costs a lot, thereby significantly increasing the fabrication of GAA MOSFET and vertically stacked GAA MOSFET, as described in Table 13.1 [35-38]. In addition, the necessity of forming these airborne channels (see three airborne channels in 'Step 6' of Figure 13.3) is

relevant for ‘fabrication of GAA MOSFET and vertically stacked GAA MOSFET’ both [30]. This can also be found in Table 13.1.

Table 13.2 Overview of disadvantages and advantages of material engineering.

Material engineering	**Disadvantage**		**Advantage**		**Location**
	Cost increase	**Yield-rate increase**	**Purpose**	**Result**	**Chapter in this book**
MOSFET	-	-	-	High I_{ON} & low I_{OFF}	1, 2
TFET	Δ (low)	-	Low Power Consumption		1, 2, 3, 4, 5, 7, 8
Hetero-Gate-Metal	O (high)	Δ (low)	Suppressing Undesirable Ambipolar Current		6
Hetero-Gate-Dielectric	O (high)	O (high)			14
Ferroelectric & NCFET	Δ (low)	Δ (low)	Low Power Consumption & High Performance		10, 11

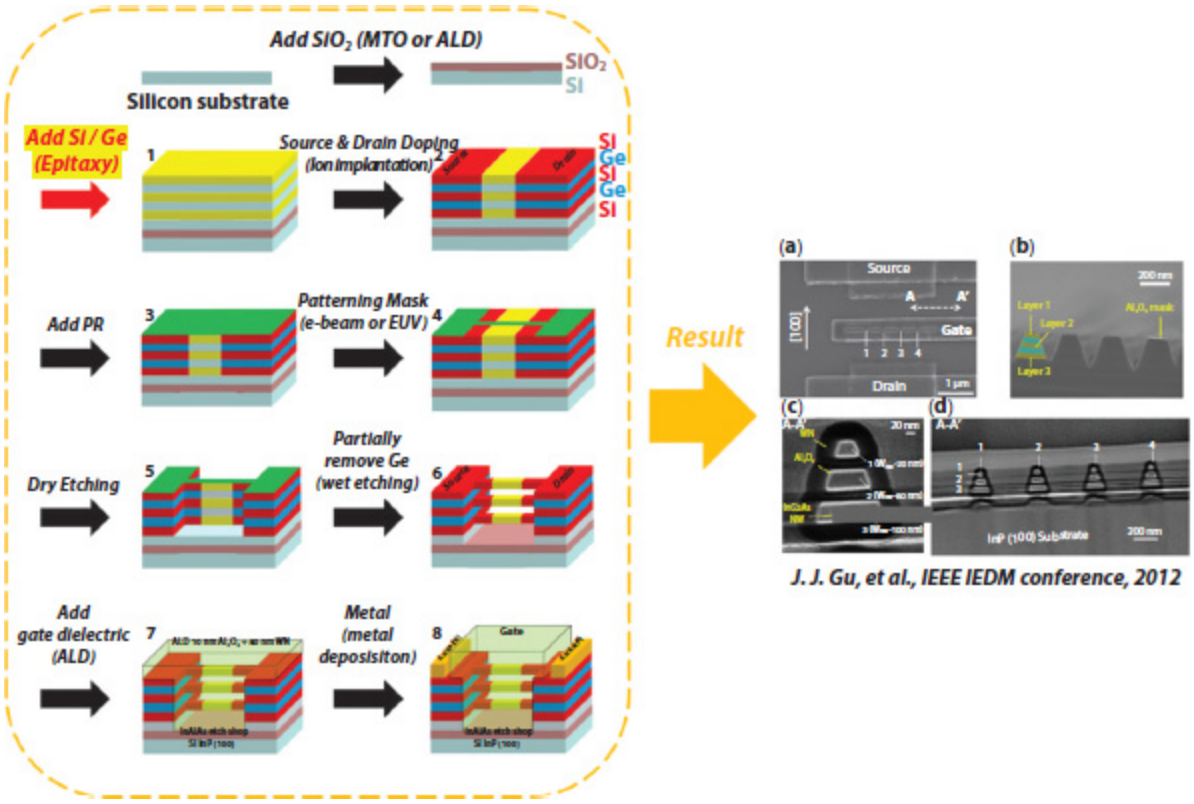

Figure 13.3 Step-by-step fabrication process of vertically stacked GAA MOSFET (MTO stands for medium-temperature oxidation, ALD stands for atomic layer deposition, EUV stands for extreme ultraviolet, and PR stands for photo resist. MTO, ALD, EUV are fabrication processes, whereas PR is material.)

The fabrication issue could be also found in material engineering. Let's take heterogate dielectric (HGD) for example, as described in Table 13.2 [39, 40]. HGD structure has been one of the promising next-generation techniques because it could suppress undesirable ambipolar current so that low off-current (I_{OFF}) and low power consumption could be simultaneously accomplished [39]. This HGD structure is particularly effective in TFET structure.

Figure 13.4 illustrates the overall fabrication process of this HGD structure (Figure 13.4 is an edited figure, the original figure can be found in the previous research done by W. Y. Choi from Sogang University [39]). Some readers may simply think that this HGD structure could be easily made since only one more material should be added in the gate dielectric layer. However, it is not that simple. In order to partially add one more SiO_2 to the

gate dielectric layer, steps ‘d’, ‘e’, and ‘f ’ should be added [Figure 13.4] [39]. In particular, step ‘d’ in Figure 13.4 means a lot. Step ‘d’ shows that one more big step (applying photoresist (PR) → exposing PR to light → applying developer) is additionally required [39]. Therefore, fabrication cost might be concomitantly increased to fabricate this HGD structure [39, 40]. In this regard, even though HGD could effectively suppress undesirable current and accomplish ultra-low power consumption, it might increase fabrication cost as well. Therefore, the manufacturer should carefully consider this trade-off issue.

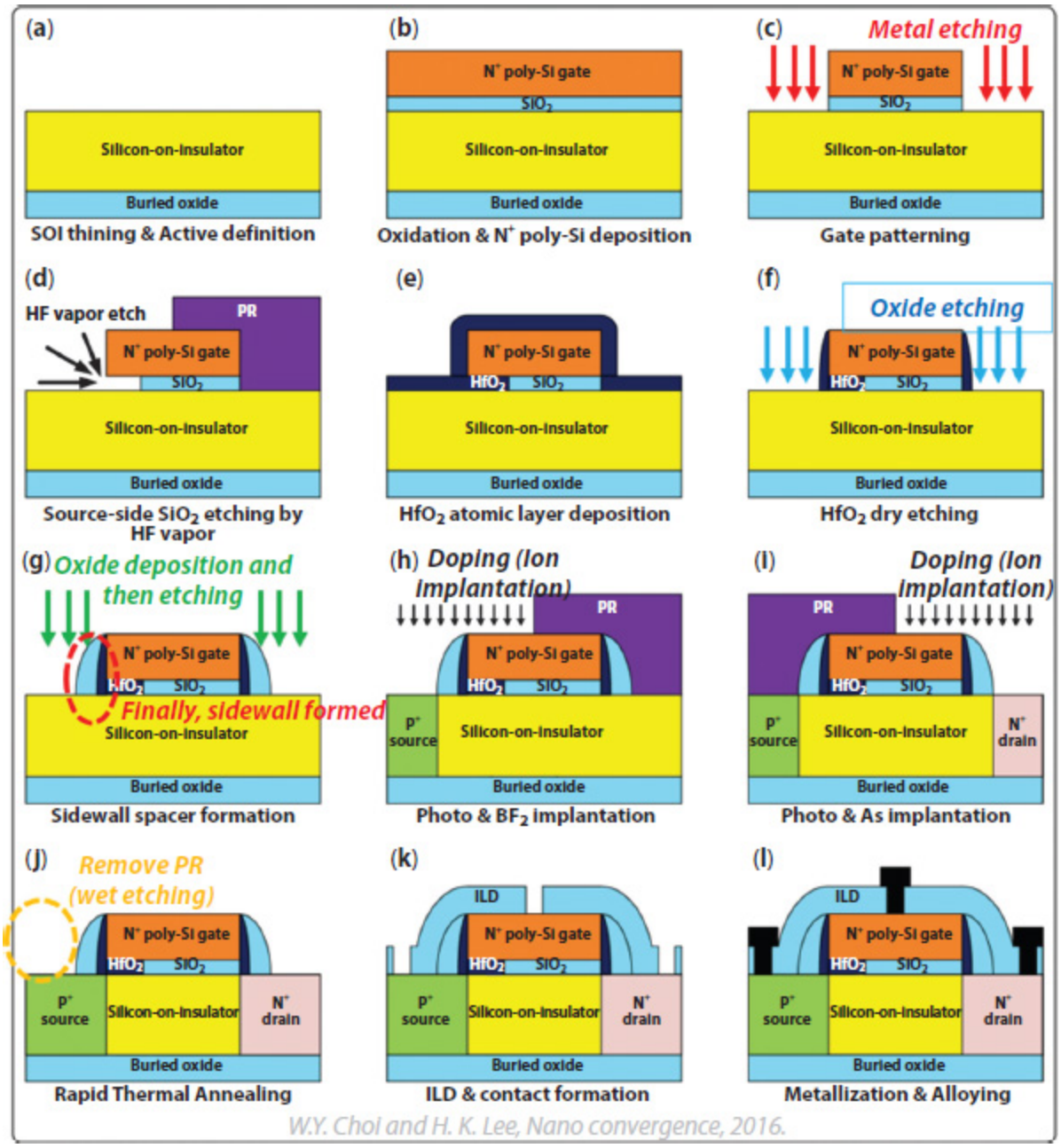

Figure 13.4 Fabrication process of heterogate dielectric structure.

13.3 Conclusion

So far, we have discussed the importance of decreasing fabrication costs while maintaining good electrical performance of transistors. In one central process unit (CPU) chip, there are countless circuits. In one circuit, there are lots of transistors. Therefore, the design of transistors should be an

engineer’s first concern and the most important consideration in the semiconductor industry.

In transistor fabrication, there are numerous steps and more than 100 processes [41]. This is because, there are both front-end (fabricating transistors, connecting transistors by metal line, sorting, etc.) and back-end processes (assembly, failure tests) [42]. Therefore, cooperation between front-end engineers and back-end engineers is paramount. Cooperation between the transistor designer and circuit designer and production department and test department are especially paramount. Of course there are several trade-off issues, so it is normal to have arguments between different departments. Take the design and test departments, for example. The design department will try to lower production costs and aim to focus on improving the performance of transistors and circuits. Therefore, the failure rate would be on the back burner (low priority). However, on the contrary, in the eyes of engineers in test department, failure rate would be one of the first considerations. This is because failure-rate and yield-rate are one of the most critical factors and measures for determining the final production cost of microchips. Therefore, cooperation between all semiconductor engineers is paramount. This philosophy is also called design technology co-optimization (DTCO) [43].

Adding one simple and cheap fabrication process (just like wet etching [Figure 13.5] and oxidation [Figure 13.6]) can critically affect the final fabrication cost and yield rate of a produced microchip. In this regard, DTCO shall be realized by all semiconductor engineers.

Of course, realizing DTCO will be not easy considering the fact that competition is getting hotter day by day in the semiconductor industry [43]. It is a well-known fact that there is constant competition for achieving success in the semiconductor industry [43]. Several semiconductor companies have competed with each other to survive [43]. Even though the cost of fabrication equipment has steadily decreased with the help of various engineers, so far reducing the production cost of microchips and producing good microchips requires a lot of effort [43].

In addition, one of the most serious limitations in transistor design is related to the physical thickness of transistors. Especially in recent 3/5-nm technology nodes, gate length (L_{gate}) has been lower than 18 nm [35–38].

The ‘12~18 nm’ gate length is already approaching its limitation. It would be hard to reduce gate length ‘endlessly’. For example, the length between two silicon (Si) atoms is known as 0.54 nm [44]. Therefore, it would be impossible to reduce gate length lower than 0.54 nm. It would be natural for us to think this, especially since transistors would be hard to be fabricated with smaller size (compared to silicon atom).

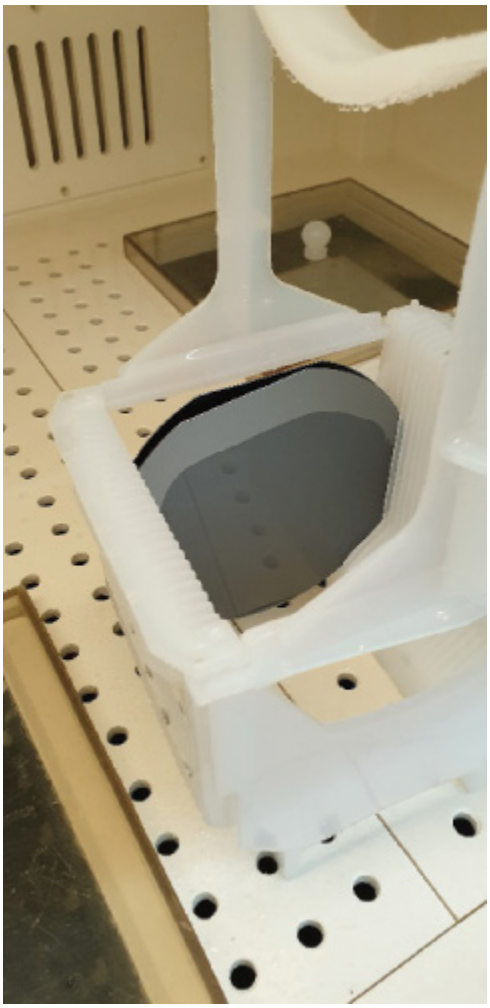

Figure 13.5 Example of Semiconductor Process: Wet Etching (This photo was taken by Prof. Young Suh Song, the main author of this chapter).

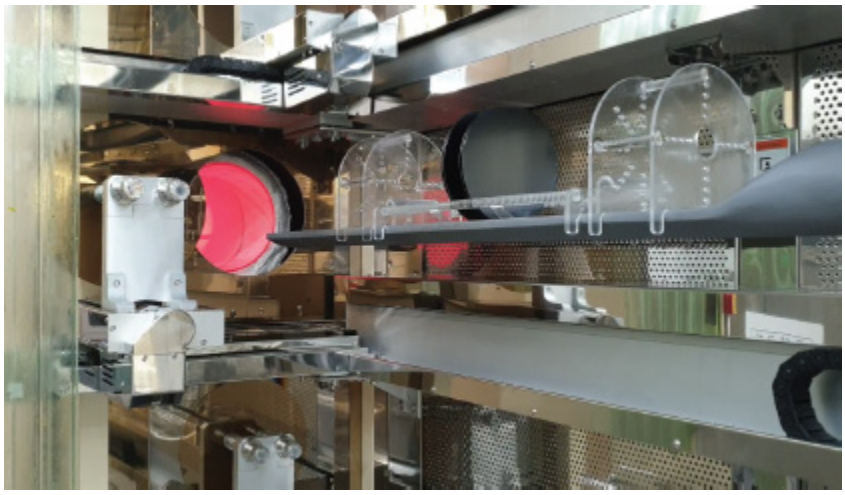

Figure 13.6 Example of Semiconductor Process: Oxidation, Chemical Vapor Deposition (CVD) (This photo was taken by Prof. Young Suh Song, the main author of this chapter).

However, there are still signs of hope. I would like to finalize this chapter and book with a quote that I heard from one of the presidents in a semiconductor company (I will not mention his/her name, but this is surely a notable episode in my personal experience):

"*Young Suh Song (2017): Sir/Madam, thank you so much for this wonderful lecture. You mentioned the GAA MOSFET as a future semiconductor technology, and you said that it can break through the limitations of semiconductors.*"

"*Young Suh Song (2017): But I have a different opinion. Anyway, we can't make a transistor smaller than an atom. In other words, it will not be possible to make a transistor smaller than 0.5 nm, which is the atomic spacing (valency length) of silicon, which is likely to act as a limit in the semiconductor industry. I'm curious what you think about this Sir/Madam.*"

(Silence Audience)

"*President A (2017): Thanks for asking this question. That's a very good question. Well, in fact, I was asked this question even 10 years ago. There were also some people who thought that the scaling of semiconductors was facing its technological limit, but we somehow managed to overcome it and have overcome so far. In this sense, I believe that '**impossible**', which may seem impossible even now, will be changed into '**possible**' instead of '**impossible**'. **The future is up to us to create**.*"

References

1. A. B. Kahng, "Scaling: More than Moore's law," in IEEE Design & Test of Computers, vol. 27, no. 3, pp. 86-87, May-June 2010, doi: 10.1109/MDT.2010.71.

2. R. R. Tummala, "Moore's Law for Packaging to Replace Moore's Law for ICS," 2019 Pan Pacific Microelectronics Symposium (Pan Pacific), 2019, pp. 1-6, doi: 10.23919/PanPacific.2019.8696409.

3. V. Moroz, X. -W. Lin and T. Dam, "Logic Block Level Design-Technology Co-Optimization is the New Moore's Law (Invited)," 2020 4th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), 2020, pp. 1-4, doi: 10.1109/EDTM47692.2020.9118018.

4. P. E. Ross, "5 Commandments [technology laws and rules of thumb]," in IEEE Spectrum, vol. 40, no. 12, pp. 30-35, Dec. 2003, doi: 10.1109/

MSPEC.2003.1249976.

5. M. J. M. Pelgrom, A. C. J. Duinmaijer and A. P. G. Welbers, “Matching properties of MOS transistors,” in IEEE Journal of Solid-State Circuits, vol. 24, no. 5, pp. 1433-1439, Oct. 1989, doi: 10.1109/JSSC.1989.572629.

6. R. H. Dennard, F. H. Gaensslen, H. -N. Yu, V. L. Rideout, E. Bassous and A. R. LeBlanc, “Design of ion-implanted MOSFET’s with very small physical dimensions,” in IEEE Journal of Solid-State Circuits, vol. 9, no. 5, pp. 256-268, Oct. 1974, doi: 10.1109/JSSC.1974.1050511.

7. W. Y. Choi, B. -G. Park, J. D. Lee and T. -J. K. Liu, “Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec,” in IEEE Electron Device Letters, vol. 28, no. 8, pp. 743-745, Aug. 2007, doi: 10.1109/LED.2007.901273.

8. Y. S. Song, S. B. Rahi, S. Tayal, A. Upadhyay, J. H. Kim, “Design Techniques for High Reliability FET by Incorporating New Materials and Electrical/thermal Co-optimization,” in Emerging Materials, 1st ed., Singapore, Springer, 2022, pp. 133-154.

9. R. S. Patti, “Three-Dimensional Integrated Circuits and the Future of System-on-Chip Designs,” in Proceedings of the IEEE, vol. 94, no. 6, pp. 1214-1224, June 2006, doi: 10.1109/JPROC.2006.873612.

10. Z. Huang, “A theoritical and practical study on logical reasoning to inversters’ yield rate,” 2011 International Conference on Business Management and Electronic Information, 2011, pp. 313-316, doi: 10.1109/ ICBMEI.2011.5916936.

11. Choi, Woo Young and Woojun Lee. “Hetero-Gate-Dielectric Tunneling Field-Effect Transistors.” IEEE Transactions on Electron Devices 57 (2010): 2317-2319.

12. P. Suveetha Dhanaselvam and A. Nithya Ananthi, “ANALYTICAL MODELING OF ELECTRIC FIELD DISTRIBUTION IN DUAL MATERIAL JUNCTIONLESS SURROUNDING GATE MOSFETS”, International Journal of VLSI design & Communication Systems (VLSICS), Vol. 5, No. 3, June 2014, pp. 83-92.

13. Mayank Shrivastava, “Why Tunnel FETs?”, COMPLIANCE, May 31, 2019. https://incompliancemag.com/article/why-tunnel-fets-part-2/

14. K. Y. Kim, Y. S. Song, G. Kim, S. Kim and J. H. Kim, “Reliable High-Voltage Drain-Extended FinFET With Thermoelectric Improvement,” in IEEE Transactions on Electron Devices, 2022, doi: 10.1109/TED.2022.3209141.

15. S. Tayal *et al.*, “Incorporating Bottom-Up Approach Into Device/Circuit Co-Design for SRAM-Based Cache Memory Applications,” in IEEE Transactions on Electron Devices, 2022, doi: 10.1109/TED.2022.3210070.

16. Y. S. Song, S. Tayal, S. B. Rahi, J. H. Kim, A. K. Upadhyay and B. -G. Park, “Thermal-Aware IC Chip Design by Combining High Thermal Conductivity Materials and GAA MOSFET,” 2022 5th International Conference on Circuits, Systems and Simulation (ICCSS), 2022, pp. 135-140, doi: 10.1109/ ICCSS55260.2022.9802341.

17. R. S. Gupta, K. Goel, M. Saxena and M. Gupta, “Physics based modeling and simulation of hetero material asymmetric gate stack epi (HEMAGASE)-MOSFET,” 2005 Asia-Pacific Microwave Conference Proceedings, 2005, pp. 4 pp.-, doi: 10.1109/APMC.2005.1606400.

18. A. K. Upadhyay, S. B. Rahi, S. Tayal, Y. S. Song, Recent progress on negative capacitance tunnel FET for low-power applications: Device perspective, Microelectronics Journal, 2022, 105583, ISSN 0026-2692.

19. K. Asano, T. Itoh, K. Kasahara, T. Ozawa and K. Ohata, “Millimeter-wave AlGaAs hetero-MIS gate InP field effect transistors,” Technical Digest., International Electron Devices Meeting, 1988, pp. 187-190, doi: 10.1109/ IEDM.1988.32786.

20. H. . -S. P. Wong *et al.*, “Metal–Oxide RRAM,” in Proceedings of the IEEE, vol. 100, no. 6, pp. 1951-1970, June 2012, doi: 10.1109/JPROC.2012.2190369.

21. N. Dharmale, S. Chaudhury, C. K. Pandey and R. Mahamune, “Determination of Structural, Electronic, Optical and Mechanical Properties of Brookite TiO2 Using Various Exchange-Correlation,” 2020

IEEE VLSI DEVICE CIRCUIT AND SYSTEM (VLSI DCS), 2020, pp. 164-170, doi: 10.1109/ VLSIDCS47293.2020.9179928.

22. R. Vaddi, R. P. Agarwal and S. Dasgupta, “Compact Modeling of a Generic Double-Gate MOSFET With Gate–S/D Underlap for Subthreshold Operation,” in IEEE Transactions on Electron Devices, vol. 59, no. 10, pp. 2846-2849, Oct. 2012, doi: 10.1109/TED.2012.2208464.

23. C. K. Pandey and S. Chaudhury, “Dual-Metal Graded-Channel Double-Gate Tunnel FETs for Reduction of Ambipolar Conduction,” 2018 IEEE Electron Devices Kolkata Conference (EDKCON), 2018, pp. 572-576, doi: 10.1109/ EDKCON.2018.8770449.

24. V. Chauhan, D. P. Samajdar, N. Bagga and A. Dixit, “A Novel Negative Capacitance FinFET With Ferroelectric Spacer: Proposal and Investigation,” in IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, vol. 68, no. 12, pp. 3654-3657, Dec. 2021, doi: 10.1109/TUFFC.2021.3098045.

25. A. Dixit, D. P. Samajdar and V. Chauhan, “Sensitivity Analysis of a Novel Negative Capacitance FinFET for Label-Free Biosensing,” in IEEE Transactions on Electron Devices, vol. 68, no. 10, pp. 5204-5210, Oct. 2021, doi: 10.1109/TED.2021.3107368.

26. M. Pavan Kumar, S. K. Gupta and M. Paul, “Corner effects in SOI-Tri gate FinFET structure by using 3D Process and device simulations,” 2010 3rd International Conference on Computer Science and Information Technology, 2010, pp. 704-707, doi: 10.1109/ICCSIT.2010.5565081.

27. F. G. Ruiz, A. Godoy, F. Gamiz, L. Donetti and C. Sampedro, “Study of the Corner Effects on Pi-Gate SOI MOSFETs,” 2007 Spanish Conference on Electron Devices, 2007, pp. 76-79, doi: 10.1109/SCED.2007.383998.

28. Baoxing Duan, Yandong Wang, Licheng Sun, Yintang Yang, “Accumulation-Mode Device: New Power MOSFET Breaking Superjunction Silicon Limit by Simulation Study”, IEEE Transactions on Electron Devices, vol.67, no.3, pp.1085-1089, 2020.

29. Y. S. Song *et al.*, “Electrical and thermal performances of omega-shaped-gate nanowire field effect transistors for low power operation”, J. Nanosci. Nanotechnol., vol. 20, no. 7, pp. 4092-4096, Jul. 2020.

30. J. J. Gu *et al.*, “III-V gate-all-around nanowire MOSFET process technology: From 3D to 4D,” 2012 International Electron Devices Meeting, 2012, pp. 23.7.1-23.7.4, doi: 10.1109/IEDM.2012.6479091.

31. N. Singh *et al.*, “High-performance fully depleted silicon nanowire (diameter /spl les/ 5 nm) gate-all-around CMOS devices,” in IEEE Electron Device Letters, vol. 27, no. 5, pp. 383-386, May 2006, doi: 10.1109/LED.2006.873381.

32. C. E. Weitzel *et al.*, “Silicon carbide high-power devices,” in IEEE Transactions on Electron Devices, vol. 43, no. 10, pp. 1732-1741, Oct. 1996, doi: 10.1109/16.536819.

33. B. J. Baliga, “Trends in power semiconductor devices,” in IEEE Transactions on Electron Devices, vol. 43, no. 10, pp. 1717-1731, Oct. 1996, doi: 10.1109/16.536818.

34. R. Gandhi, Z. Chen, N. Singh, K. Banerjee and S. Lee, “Vertical Si-Nanowire n -Type Tunneling FETs With Low Subthreshold Swing (≤50 mV/decade) at Room Temperature,” in IEEE Electron Device Letters, vol. 32, no. 4, pp. 437-439, April 2011, doi: 10.1109/LED.2011.2106757.

35. P. D. Ye *et al.*, “GaAs MOSFET with oxide gate dielectric grown by atomic layer deposition,” in IEEE Electron Device Letters, vol. 24, no. 4, pp. 209-211, April 2003, doi: 10.1109/LED.2003.812144.

36. S. Bangsaruntip *et al.*, “High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling,” 2009 IEEE International Electron Devices Meeting (IEDM), 2009, pp. 1-4, doi: 10.1109/IEDM.2009.5424364.

37. C. -J. Su, T. -I. Tsai, Y. -L. Liou, Z. -M. Lin, H. -C. Lin and T. -S. Chao, “Gate-All-Around Junctionless Transistors With Heavily Doped Polysilicon Nanowire Channels,” in IEEE Electron Device Letters, vol. 32, no. 4, pp. 521-523, April 2011, doi: 10.1109/LED.2011.2107498.

38. M. V. Fischetti and S. E. Laux, “Monte Carlo simulation of transport in technologically significant semiconductors of the diamond and zinc-blende structures. II. Submicrometer MOSFET’s,” in IEEE Transactions on Electron Devices, vol. 38, no. 3, pp. 650-660, March 1991, doi: 10.1109/16.75177.

39. W. Y. Choi and H. K. Lee, “Demonstration of hetero-gate-dielectric tunneling field-effect transistors (HG TFETs),” Nano Convergence, vol. 3, no. 13, June 2016, doi: 10.1186/s40580-016-0073-y.

40. Y. S. Song, J. H. Kim, G. Kim, H. -M. Kim, S. Kim and B. -G. Park, “Improvement in Self-Heating Characteristic by Incorporating Hetero-Gate-Dielectric in Gate-All-Around MOSFETs,” in IEEE Journal of the Electron Devices Society, vol. 9, pp. 36-41, 2021, doi: 10.1109/JEDS.2020.3038391.

41. L. N. Sun, T. M. H. Lee, Z. C. Yang and G. Z. Yan, “Fabrication of Sub-100-nm silicon nanowire devices on SOI wafer by CMOS compatible fabrication process,” 2010 IEEE 5th International Conference on Nano/ Micro Engineered and Molecular Systems, 2010, pp. 971-974, doi: 10.1109/ NEMS.2010.5592606.

42. Q. Yunrui, “Front-End and Back-End Separation for Warehouse Management System,” 2018 11th International Conference on Intelligent Computation Technology and Automation (ICICTA), 2018, pp. 204-208, doi: 10.1109/ ICICTA.2018.00053.

43. A. Asenov *et al.*, “Variability Aware Simulation Based Design-Technology Cooptimization (DTCO) Flow in 14 nm FinFET/SRAM Cooptimization,” in IEEE Transactions on Electron Devices, vol. 62, no. 6, pp. 1682-1690, June 2015, doi: 10.1109/TED.2014.2363117.

44. Lap Van Dao *et al.*, “Time Resolved and Time Integrated Photoluminescence for Study of Optical Properties of Silicon Quantum Dots,” Conference on Optoelectronic and Microelectronic Materials and Devices, 2004., 2004, pp. 369-372, doi: 10.1109/COMMAD.2004.1577567.

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Index

ambipolar effect 37
analog 98
analytical modeling 79
atomistic modeling 78

bandgap effect 41
biosensor 83
body effect 4
Boltzmann’s tyranny 1
BTBT 2, 3, 4, 9, 11
bulk MOSFETs 17

carbon nanotube 17
CMOS 12, 14, 20, 21
compact model 83
cost 221
cost function 238

delay 154, 170
depletion Width 9
DGSOI 17, 20
DIBL 1, 5, 6, 11, 12, 14
digital circuits 220

electric field 11,

electrical parameters 108
electrons 181, 241

fabrication 14
ferroelectric 279, 281
FinFET 1, 17, 279, 282, 283
Fowler–Nordheim (FN) 7

GAA MOSFET 279, 280, 284
gate metal material technique 279
gate-all-around transistors 1, 17
GIDL 1, 2, 9, 10, 11
group III-V materials 33
group IV materials 34

halo Doping 11, 14
hetero-gate structure 279
hetero-structures 34
holes 241, 266, 267

interface engine 249
interface trap 119
intrinsic delay 40

junctionless transistor 279

Landau-Khalantnikov 18
leakage 7, 10, 11
line TFET 170–173
logic gates 12, 13

low power 280, 282

memory 13,
memory window 124
metal oxide semiconductor field effect transistors 279
mobility 99, 100, 174
Moore’s Law 1
MOS Transistors 1, 2
MOSFETs 5–9, 31–34
MTCMOS 12
multi-gate transistors 1

Nanosheet 188, 190
nanowire 1
NCFET 279, 281, 283
negative capacitance effect 17
NMOS 14, 15
NSFET 279, 280

OFF state 2, 12
OFF state leakage 11
ON state 12
optimization 14, 17
oxide material technique 279
oxide tunneling 2

PDA 13, 20
PMOS 14, 15
PN Junction 2, 3, 4

power consumption 65
pseudo-NMOS 20
punch through 10
punch-through 14

radiation effect 266
retrograde Doping 11, 14
RF FOM 98

scaling 1, 11, 12, 13
SCEs 11, 14
semiconductor 13
short channel effect 83, 86
SOI 1, 17
SRAM 136–142
stacked transistors 17
stacking effect, 12
structural engineering 279
subthreshold 1
subthreshold leakage 2, 4, 6, 12
subthreshold slope 6, 14, 19
subthreshold technology 2, 13
subthreshold transistor 1, 12, 13, 14, 17
supply voltage 209, 212, 217
surface potential 45

temperature 6, 7, 8, 13
temperature dependence 118

TFET 279, 281
TFET 279, 283, 284
TFETs 1, 15, 17
thermal voltage 6
thermodynamic 242
thin film transistors 1
threshold, voltage 4, 5, 6, 10, 11, 12, 19
tunneling 2, 7, 8
ultra low power 279, 282
voltage 13
VTCMOS 12
Vth Roll-Off 6

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